

Compal Confidential

STORM2 M/B Schematic

LA-E291P

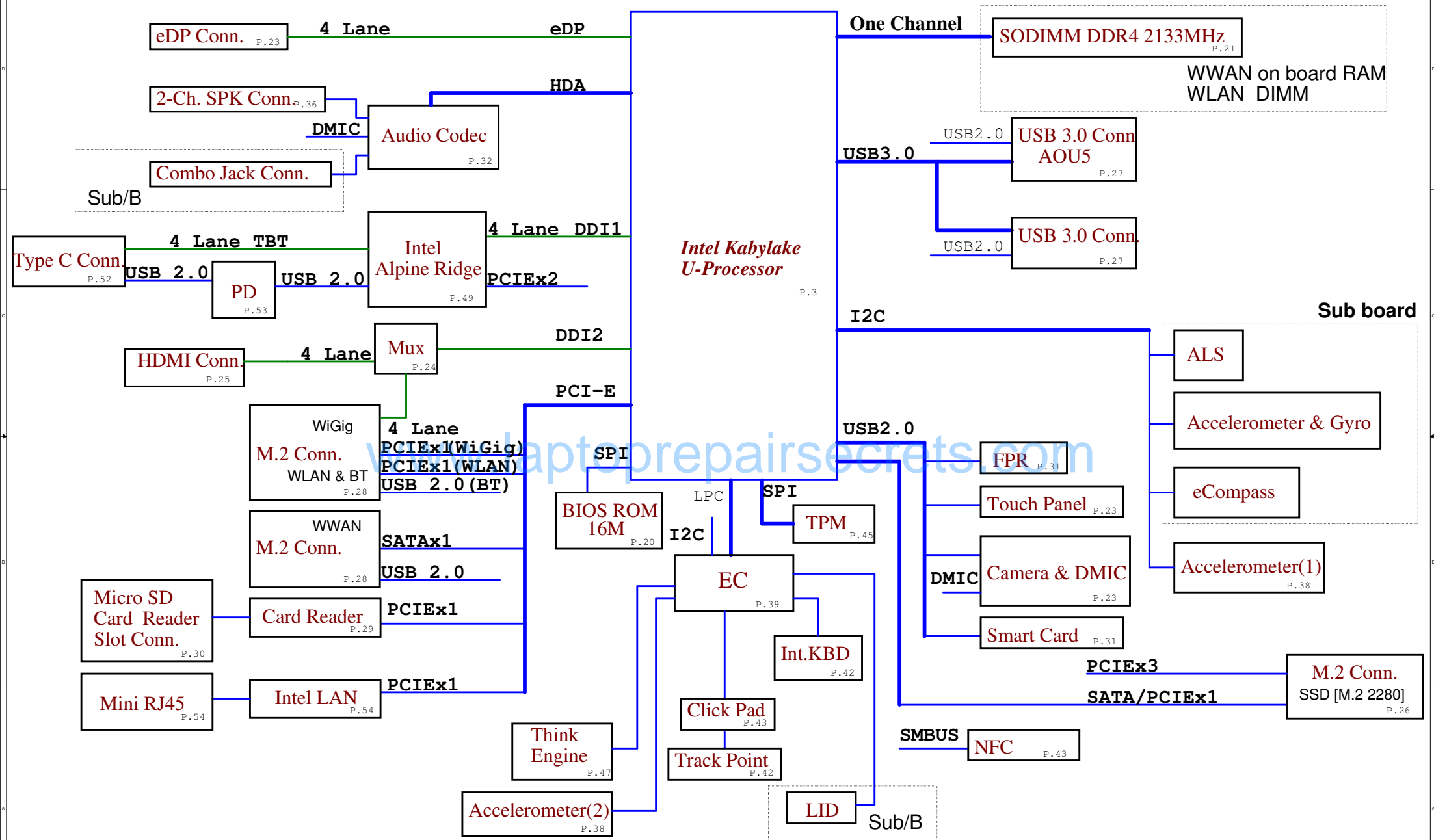
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Rev: 0.3_B

2016.09.01

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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STORM 2 Block-Diagram



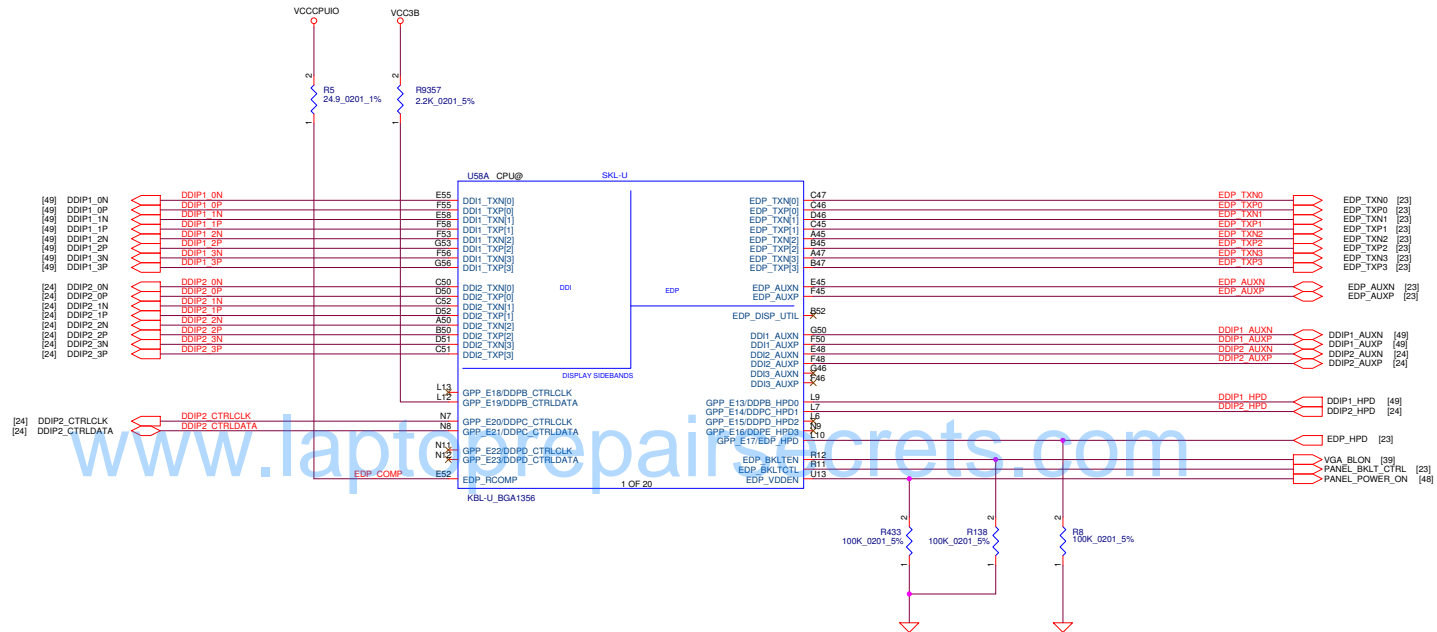


TABLE : Functional Strap

DDPB_CTRLDATA

HIGH Port B is detected.
LOW Port B is not detected.

DDPC_CTRLDATA

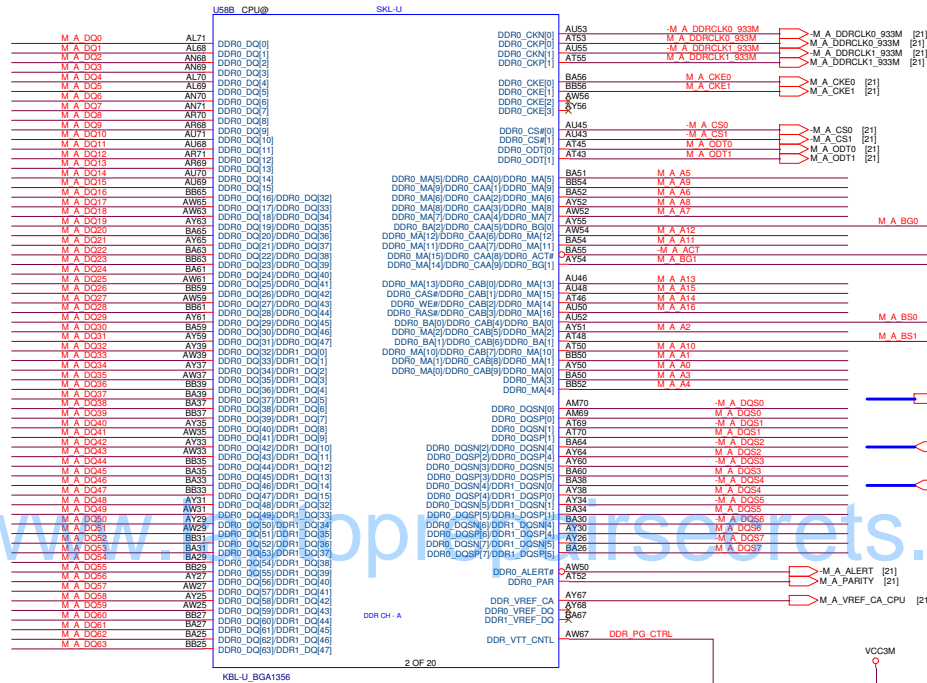
HIGH Port C is detected.
LOW Port C is not detected.

[21] M_A_DQ[63:0]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AT22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSN[1]	DDR0_DQSN[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]

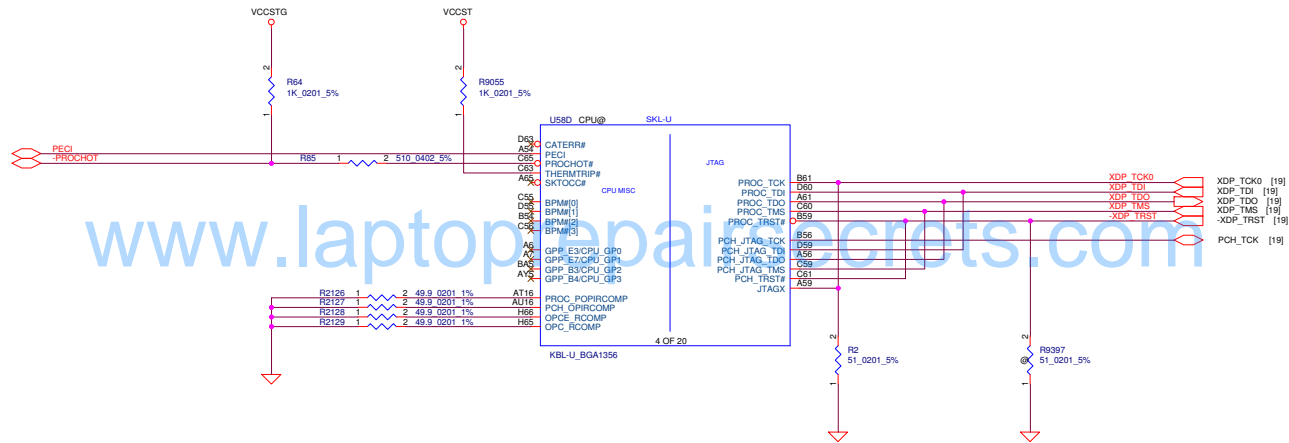
LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BA48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BA44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

[40] PEGI
[39,40,64,66] -PROCHOT



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SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

SPI0_MISO (JTAG ODT Diable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

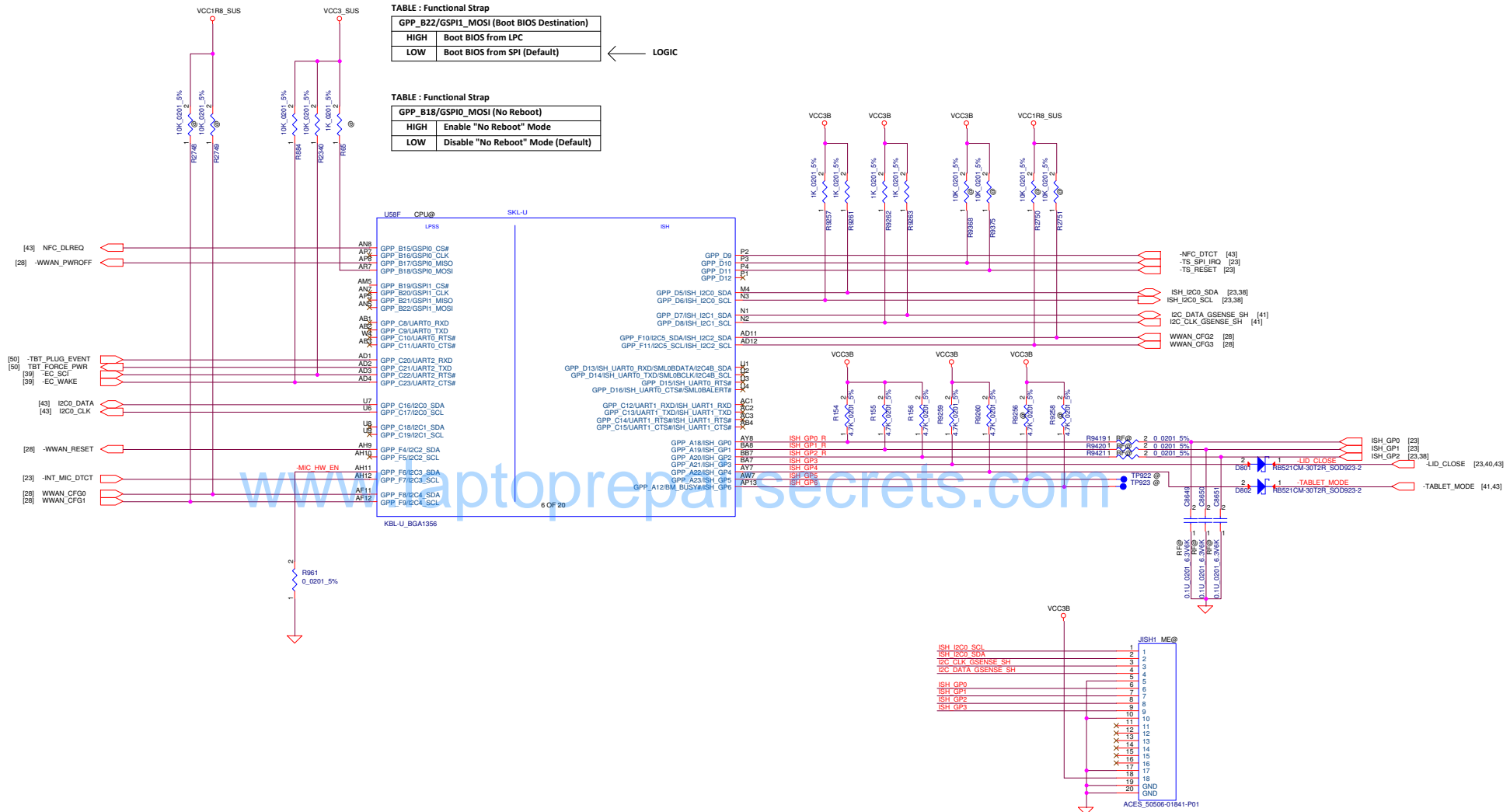
← LOGIC

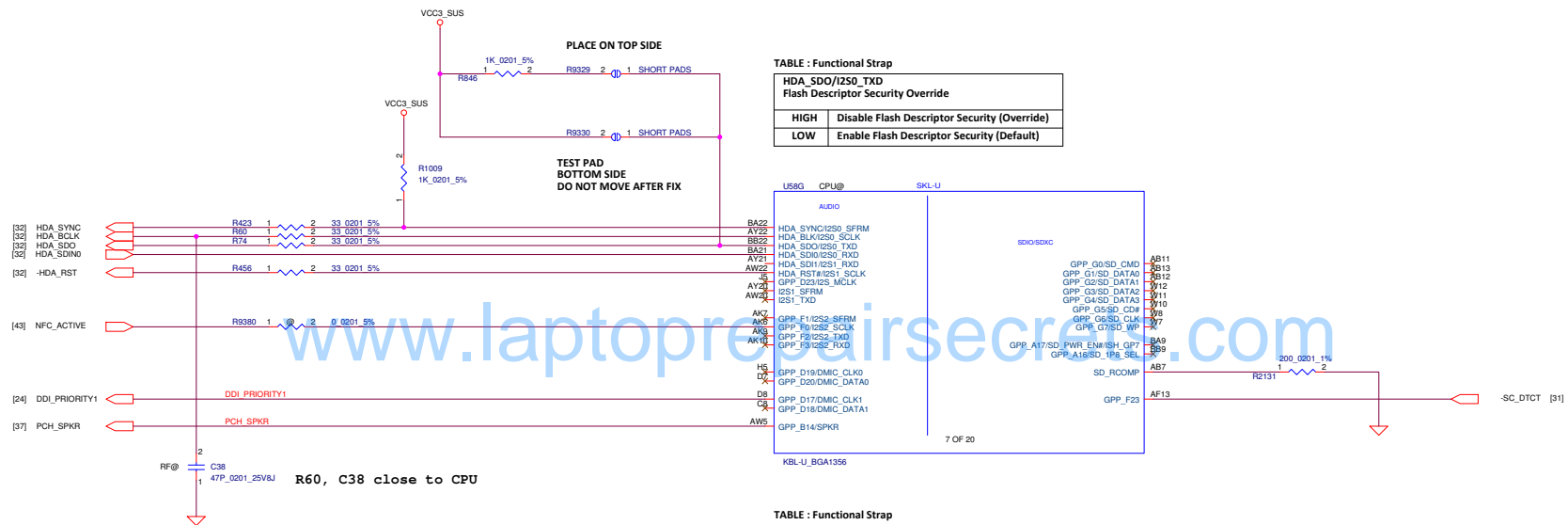


SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

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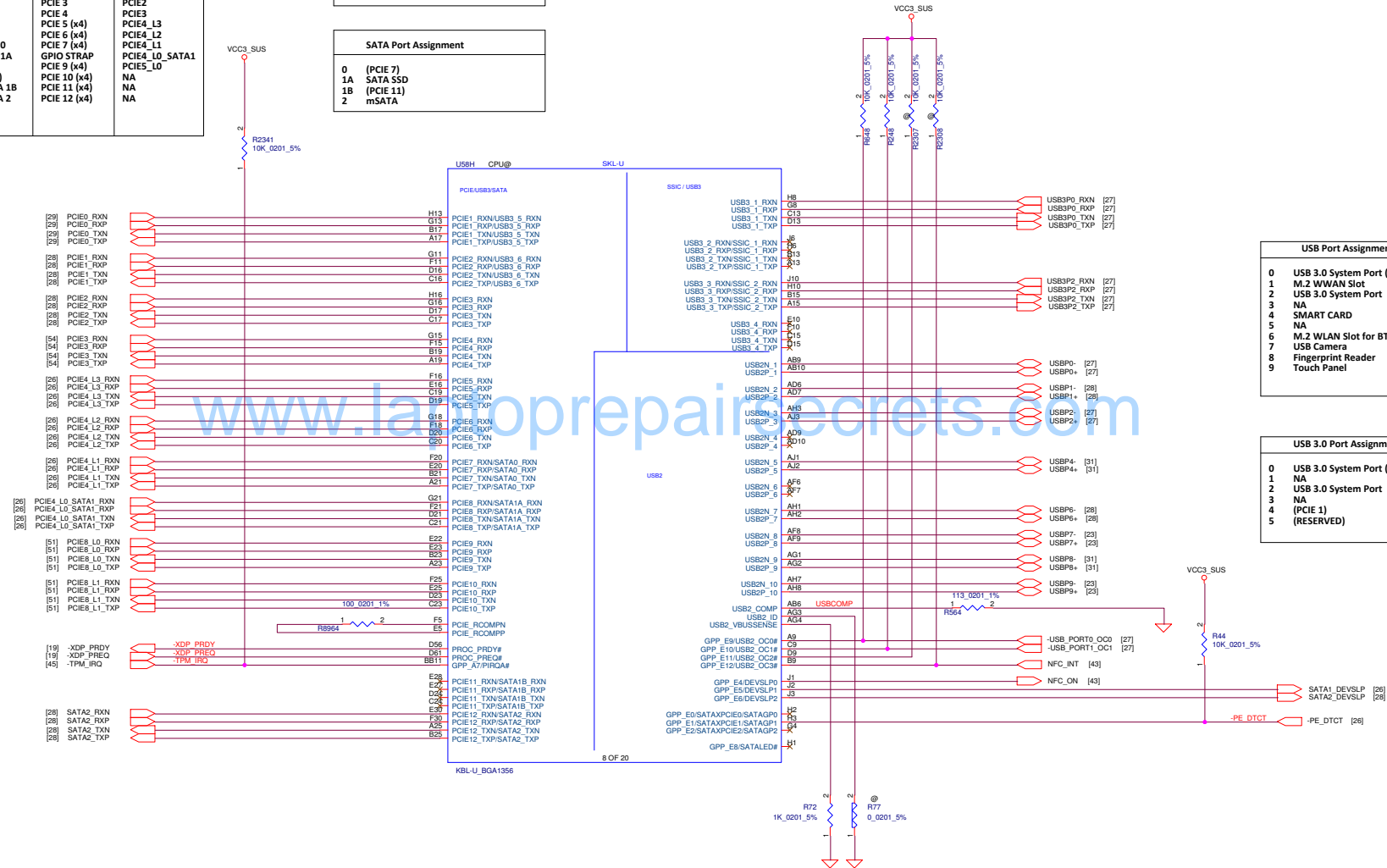
Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	SSIC	SSIC
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	USB3 6	USB3P5
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	NA
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	NA
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	NA

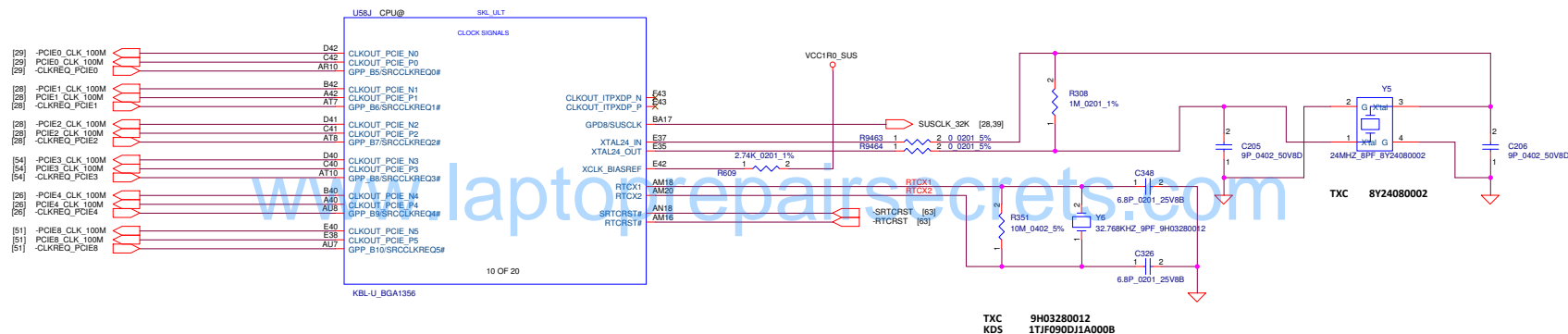
PCIe Port Assignment	
0	Media Card Controller
1	M.2 WLAN Slot Port 1 for WiGig
2	M.2 WLAN Slot Port 0 for WLAN
3	GBE PHY
4 (x4)	PCIE SSD
8 (x2)	Thunder bolt

SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD
1B	(PCIE 11)
2	mSATA

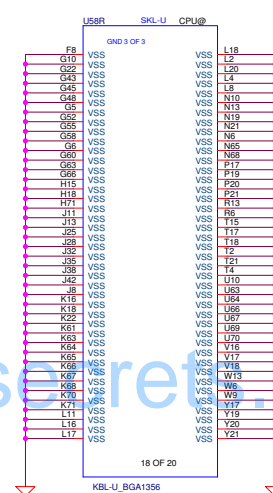
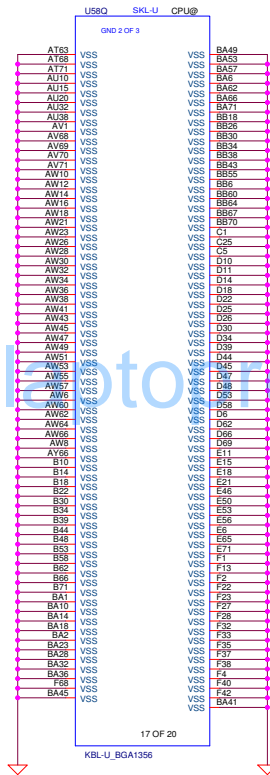
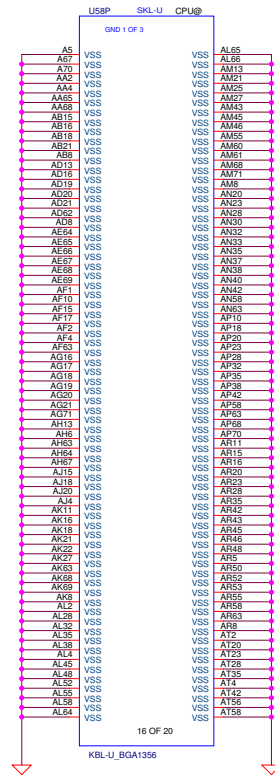
USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot
2	USB 3.0 System Port
3	NA
4	SMART CARD
5	NA
6	M.2 WLAN Slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	NA
2	USB 3.0 System Port
3	NA
4	(PCIE 1)
5	(RESERVED)

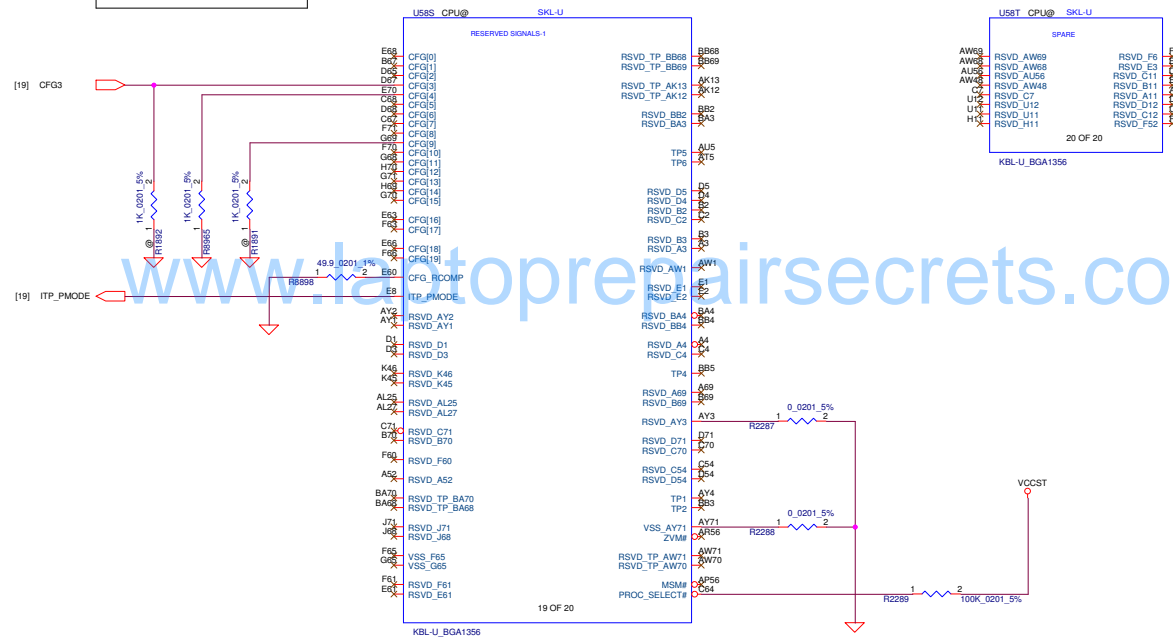


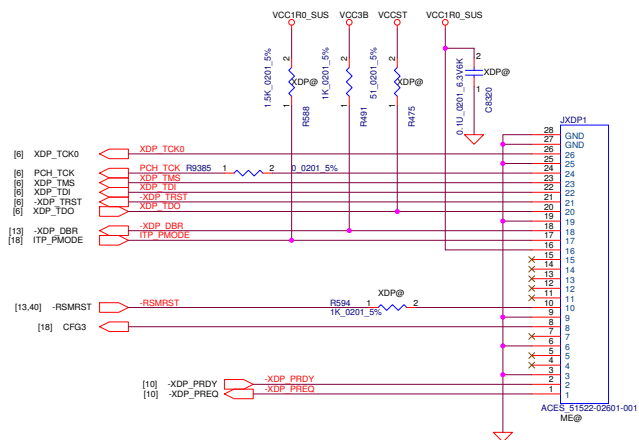


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<p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall</p>
<p>CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden</p>
<p>CFG4 : eDP Enable 1 : Disabled 0 : Enabled</p>
<p>CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled</p>



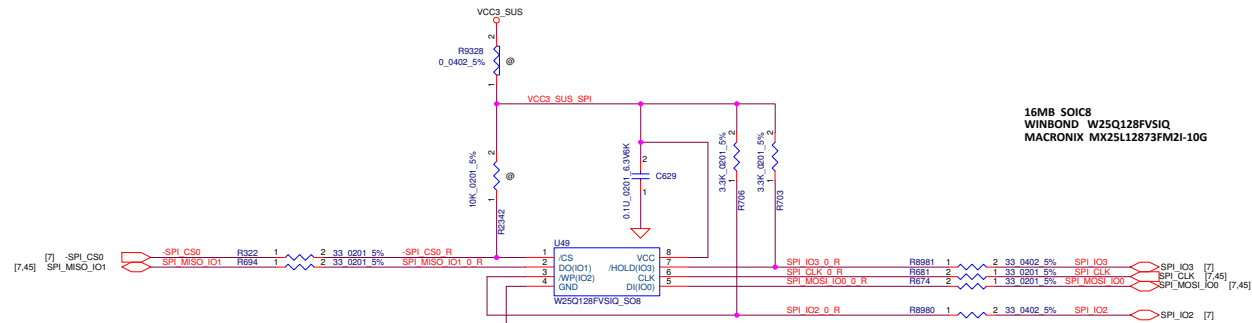


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TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R2559	ASM	NO_ASM
Page 18	R1982	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

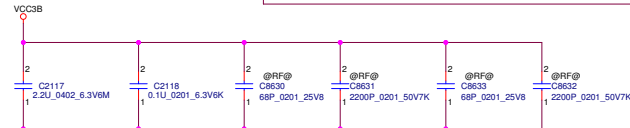
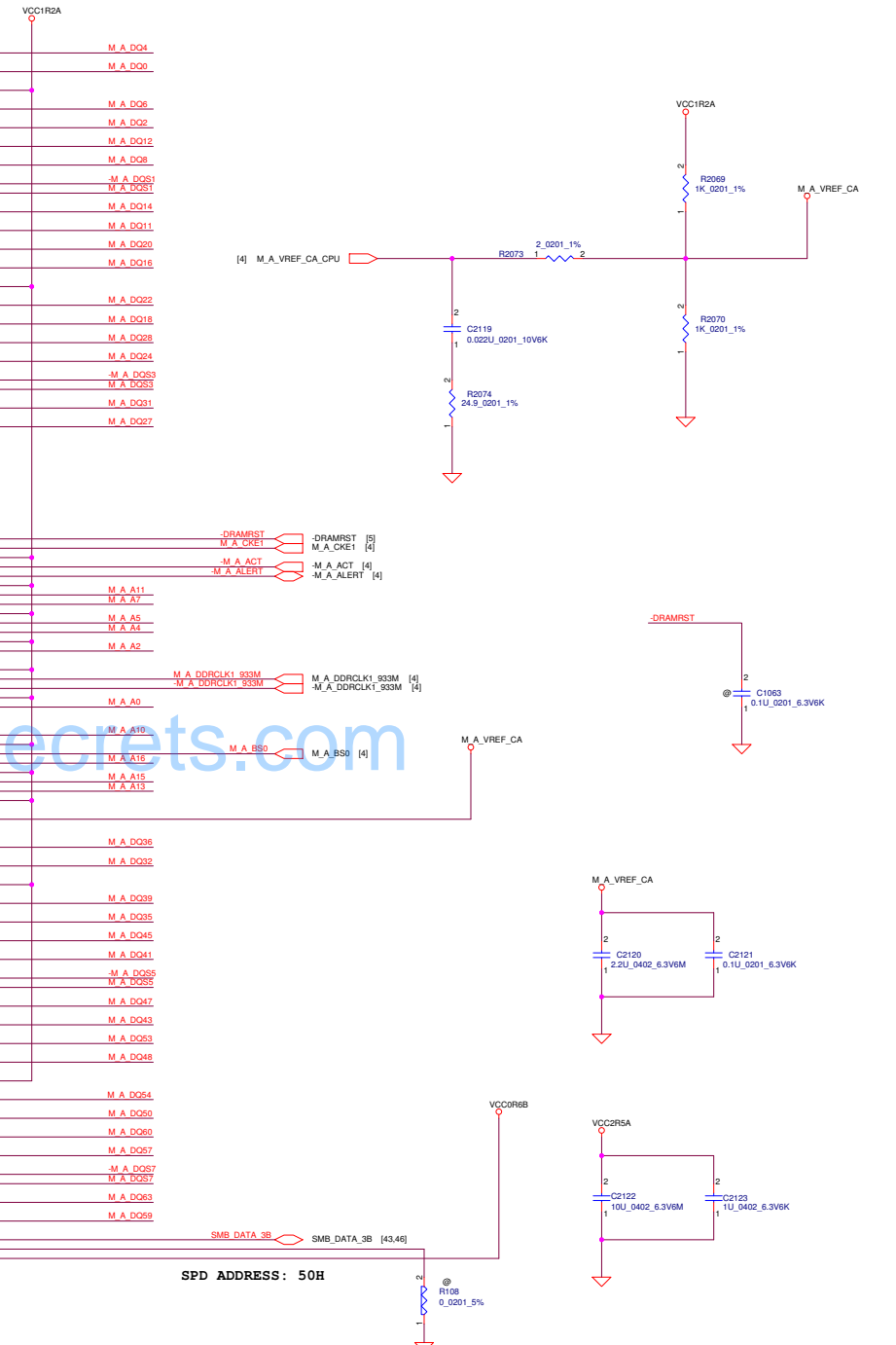
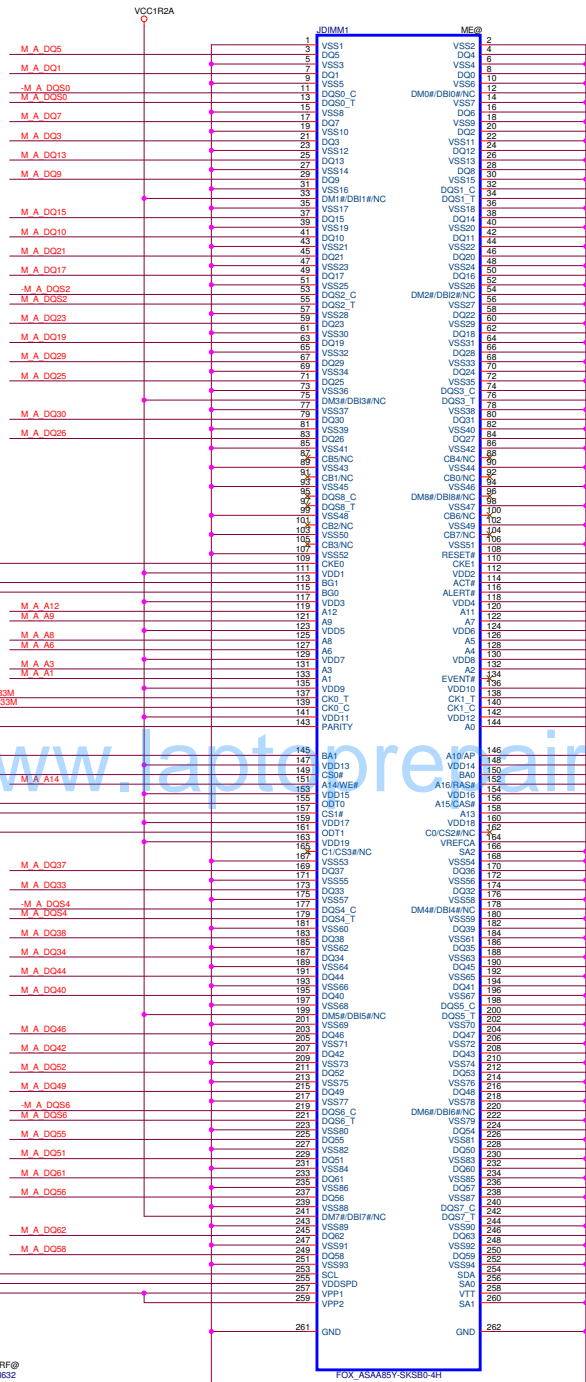
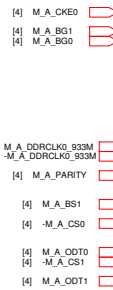
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	XDP CONNECTOR
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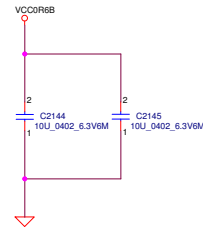
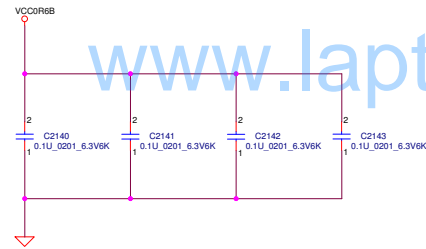
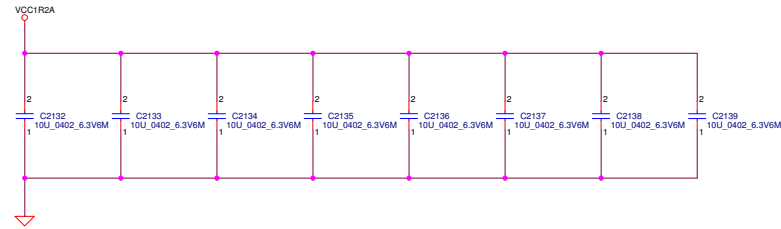
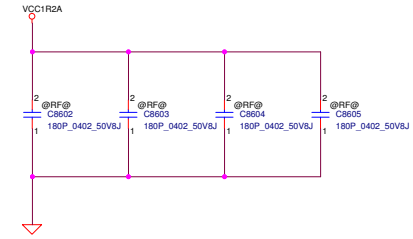
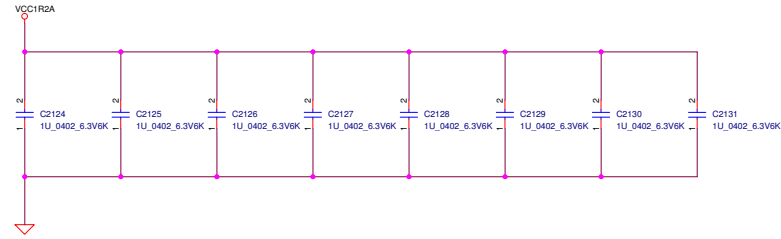
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TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

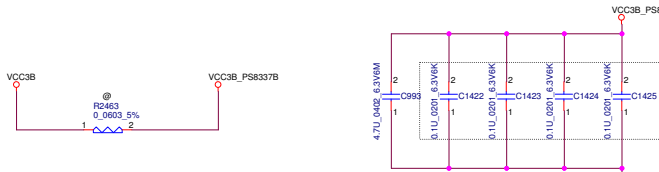


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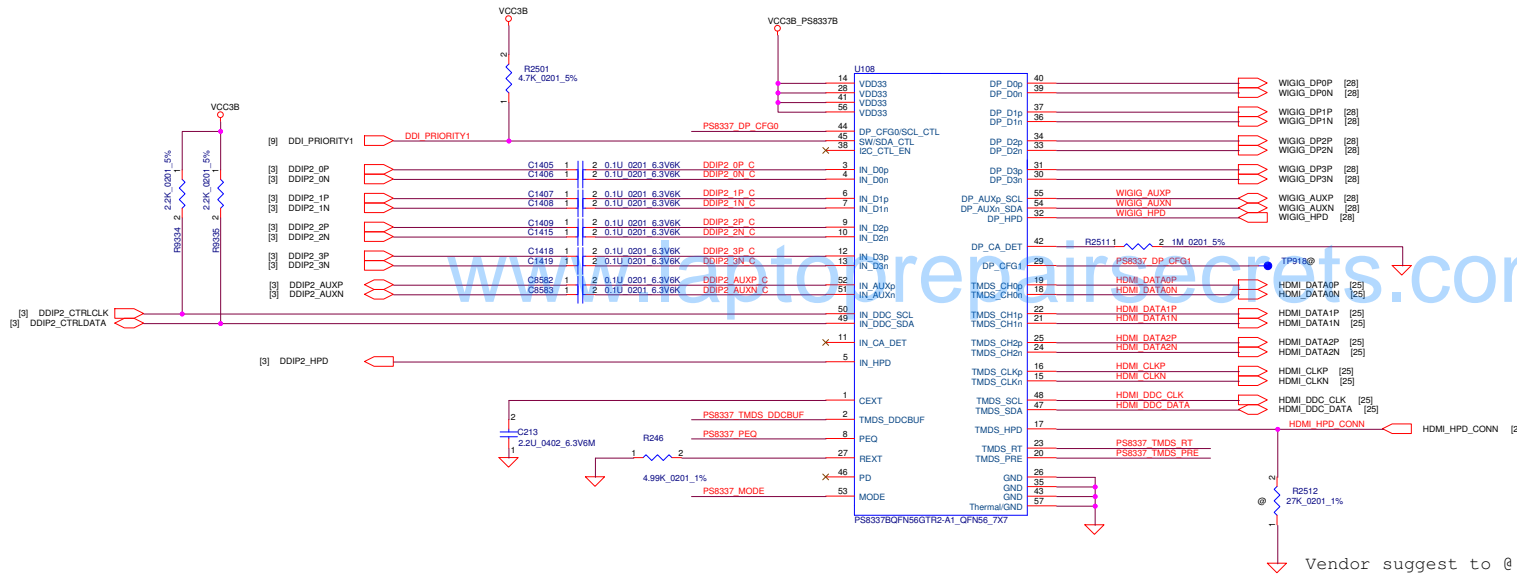
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	DDR4 SO DIMM CHANNEL-A (2/2)
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Place 0.1uF caps near each VDD33 pin of PS8337

TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged
H TMDS Port has higher priority when both ports are plugged



TMDS DDCBUF (INT PD)	R1876	R1898
DDC Active Buffer	ASM	NO_ASM
DDC Pass Through w/ PU	ASM	ASM
DDC Pass Through w/o PU	NO_ASM	NO_ASM

LOGIC

PEQ (INT PD)	R1875	R1897
HEQ 15dB	ASM	NO_ASM
LLEQ 5dB	ASM	ASM
LEQ 12dB	NO_ASM	NO_ASM

LOGIC

TMDS PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

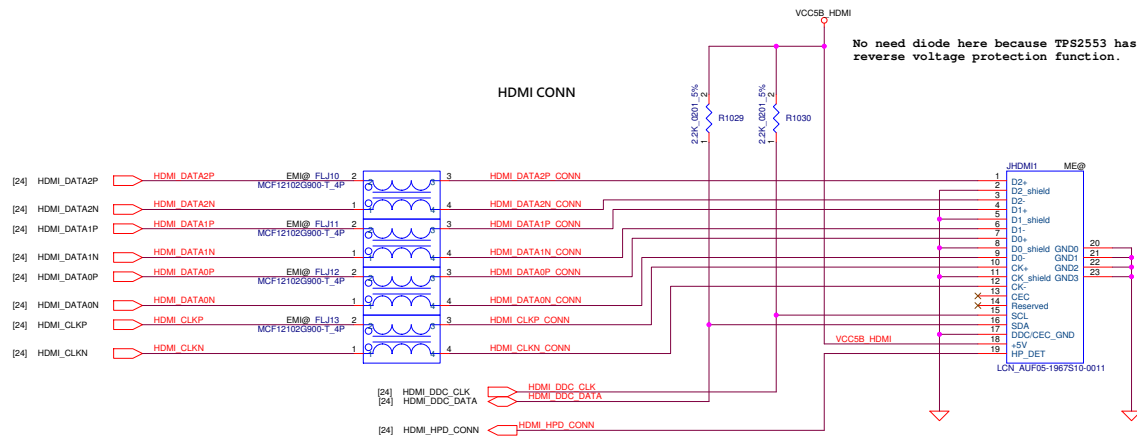
LOGIC

MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

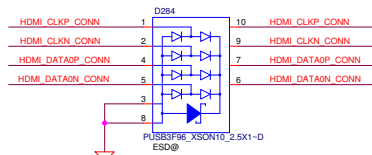
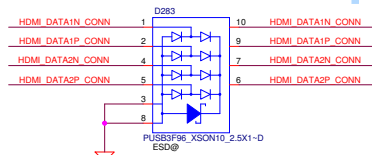
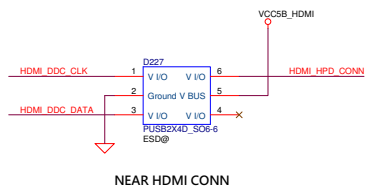
LOGIC

TMDS RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

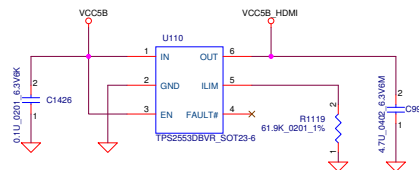
LOGIC



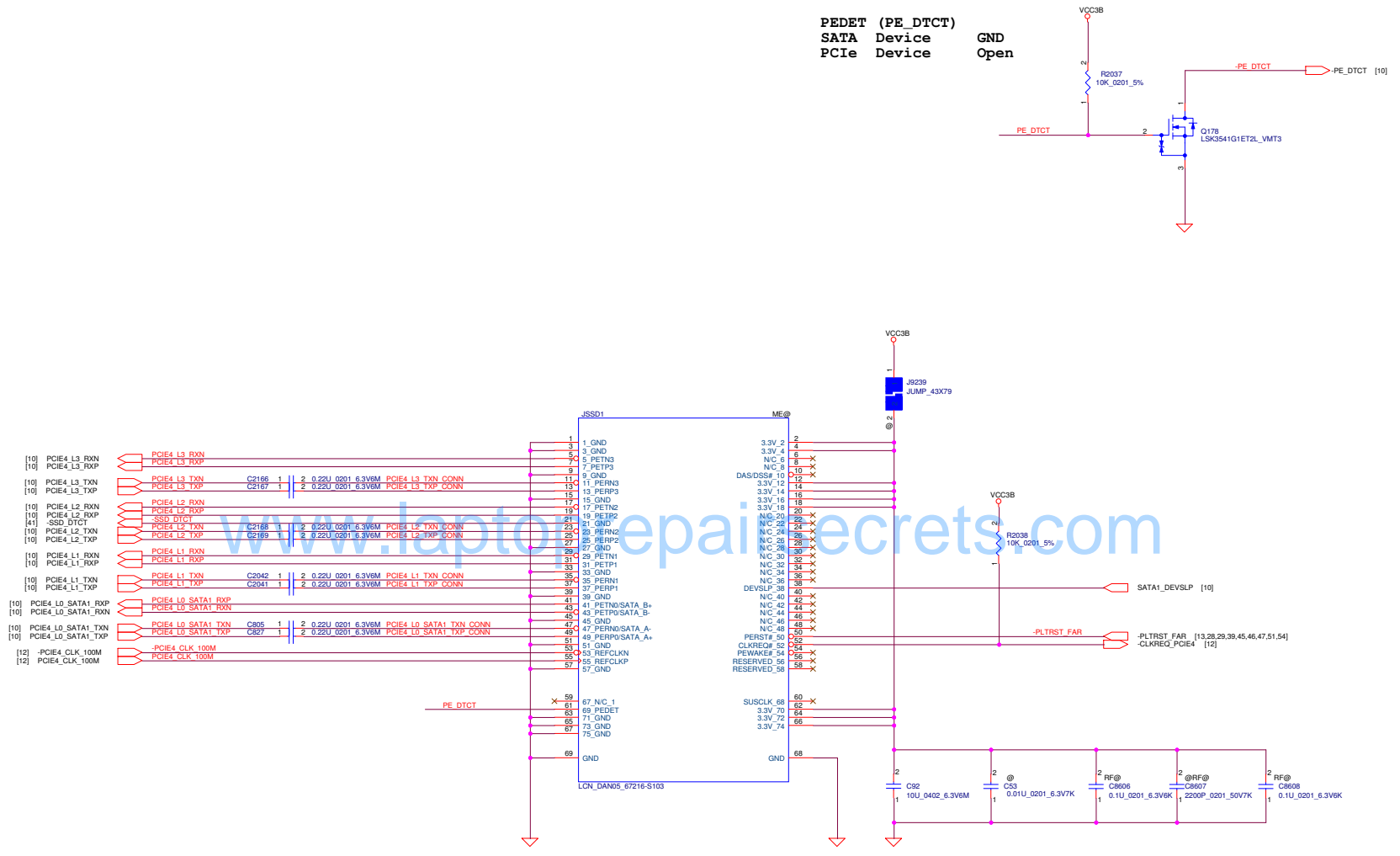
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Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA



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PEDET (PE_DTCT)
SATA Device
PCIe Device

GND
Open

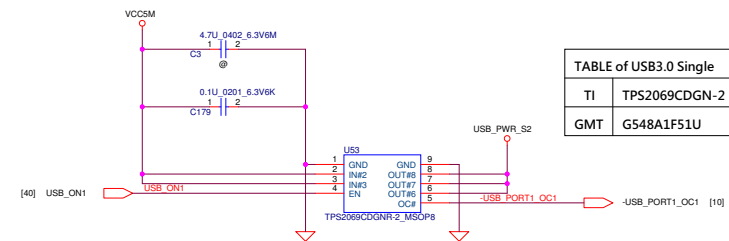
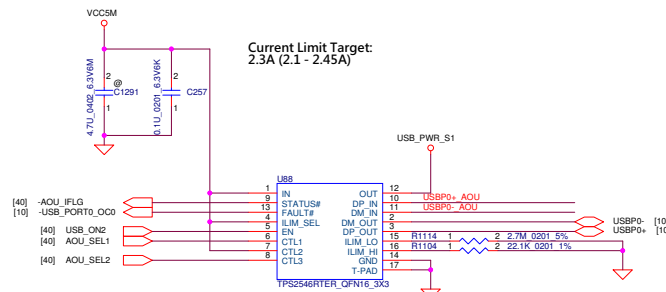
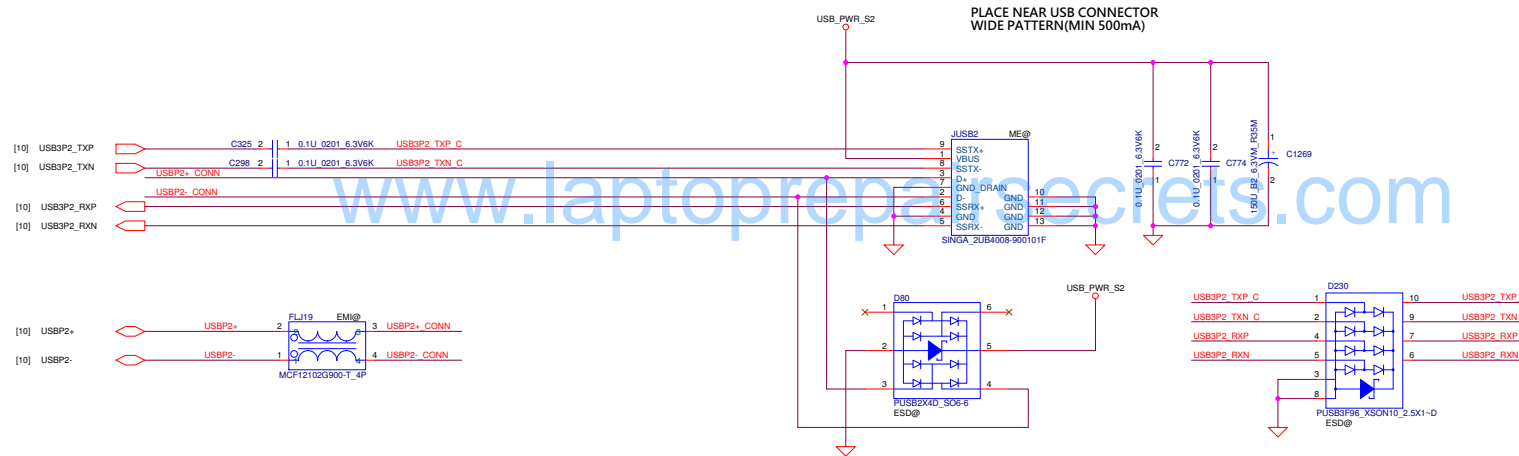
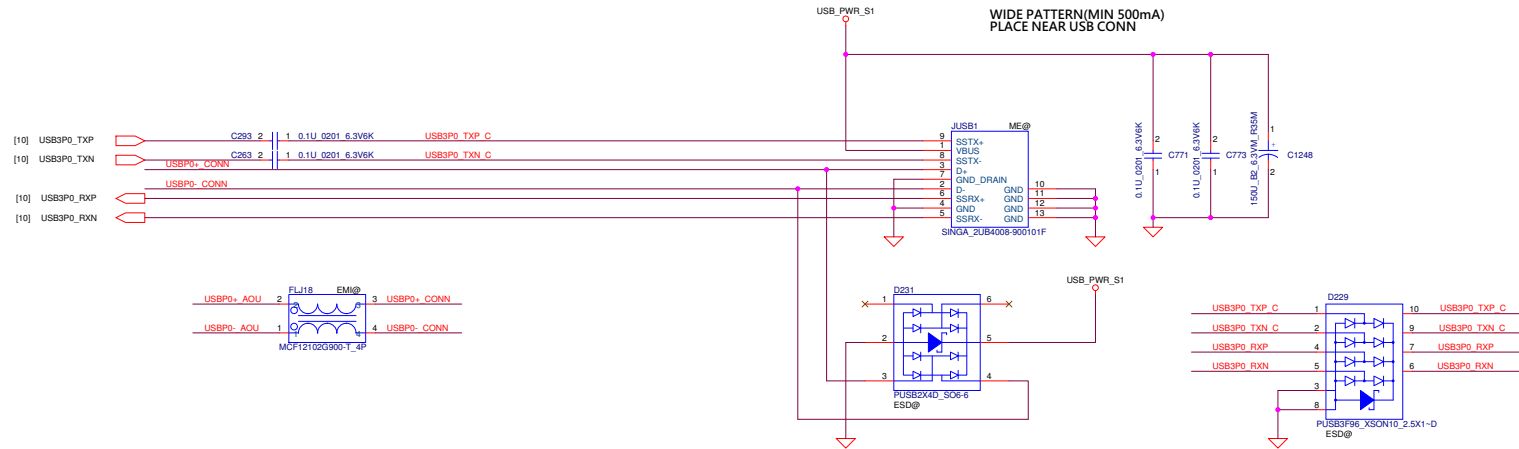
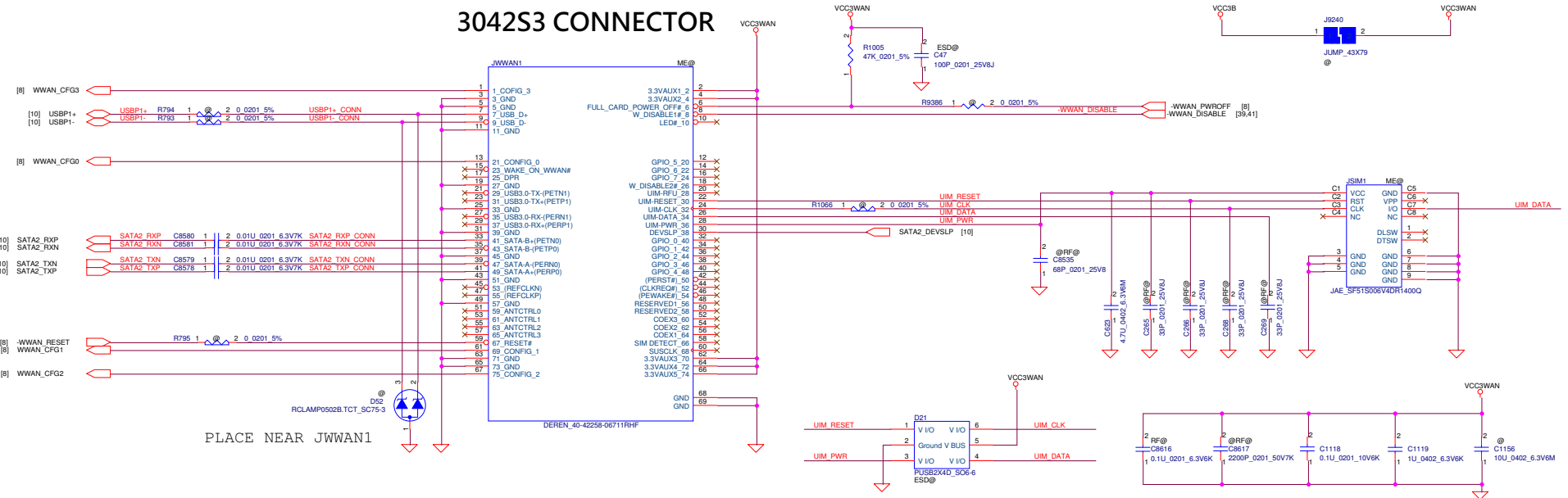


TABLE of USB3.0 Single	
TI	TPS2069CDGN-2
GMT	G548A1F51U

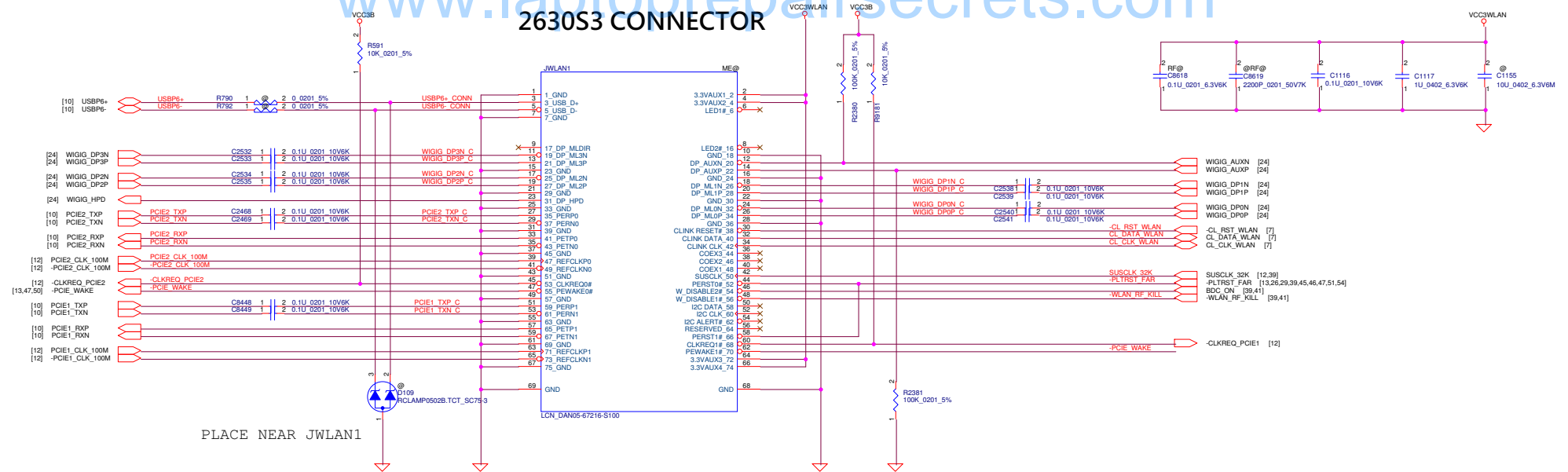
TYPE-B M.2 CARD FOR WWAN

3042S3 CONNECTOR



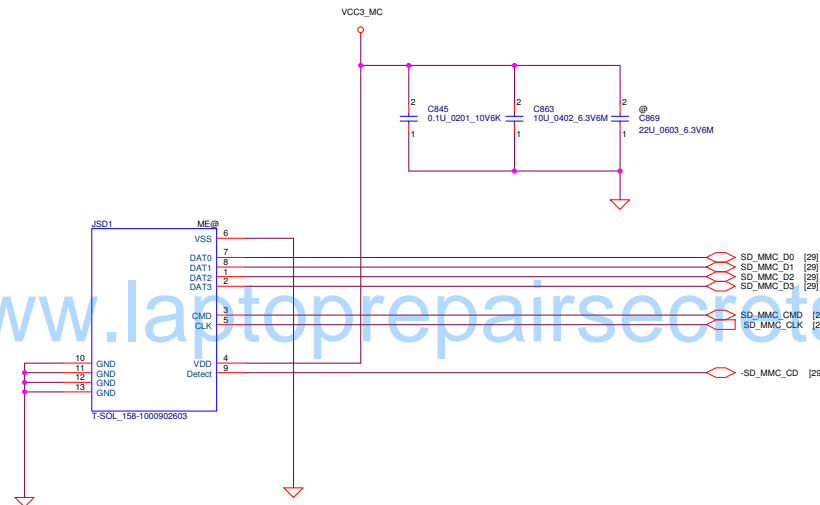
TYPE-A M.2 CARD FOR WLAN / Bluetooth / WiGig

2630S3 CONNECTOR

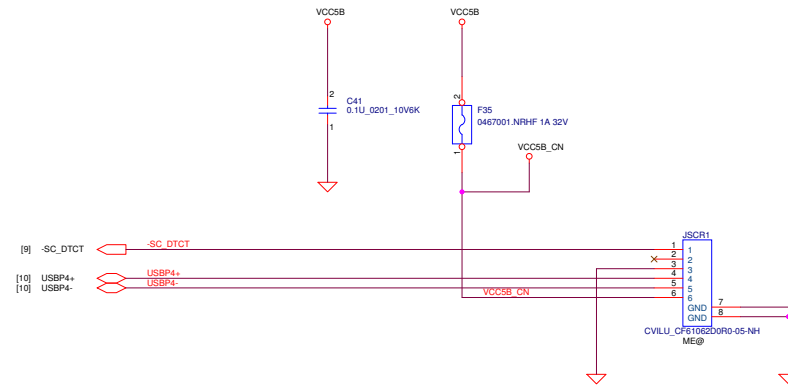


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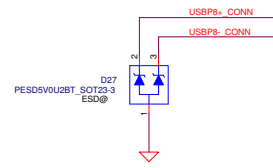
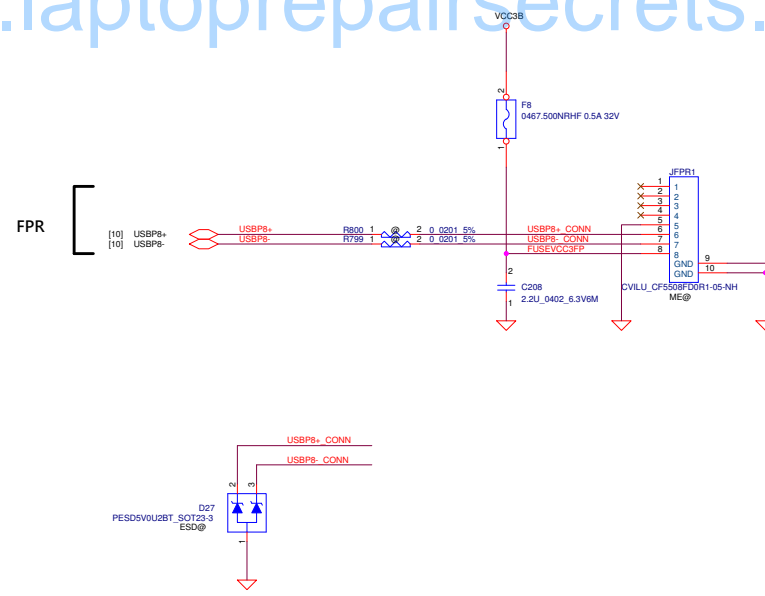
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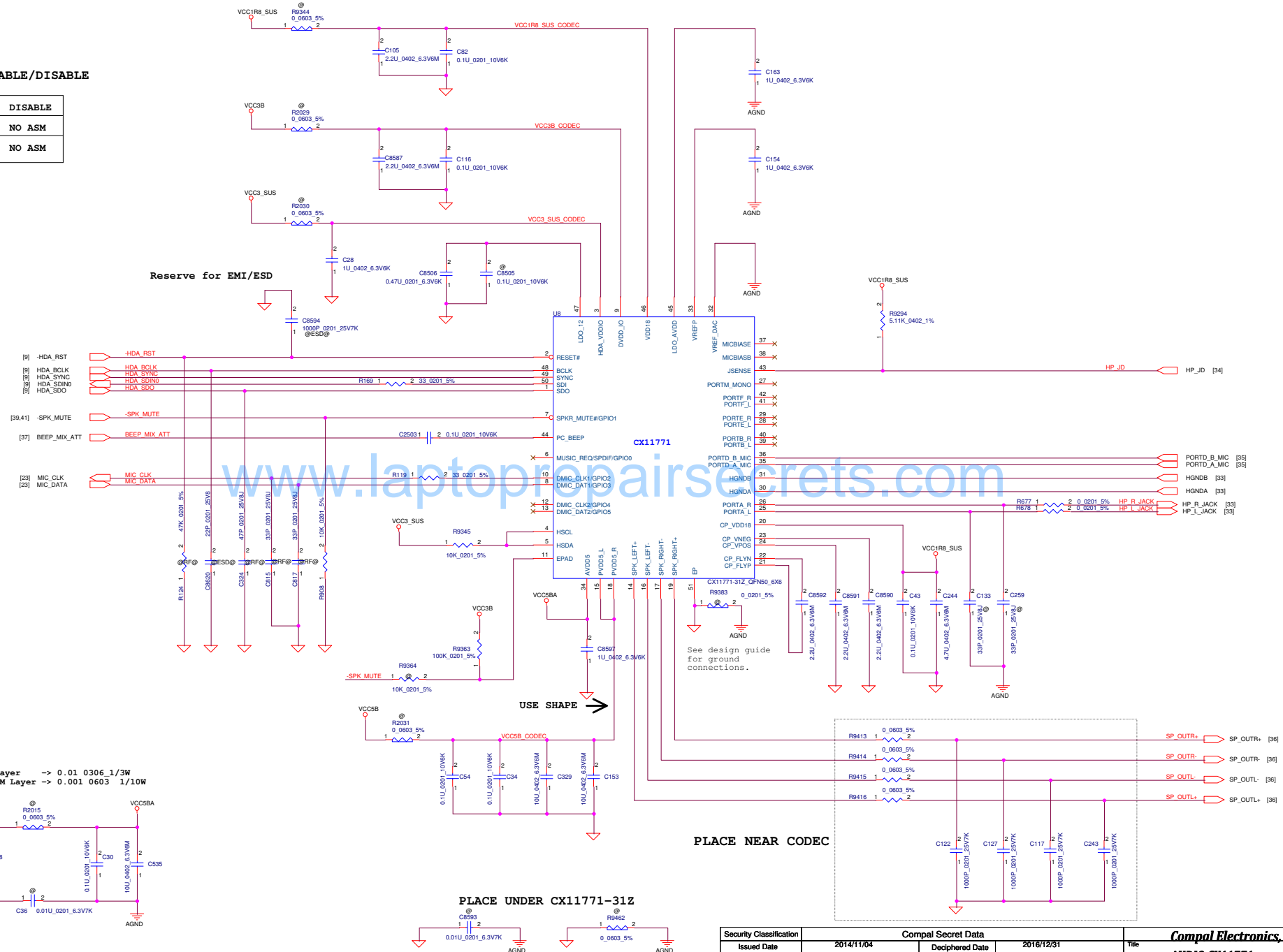


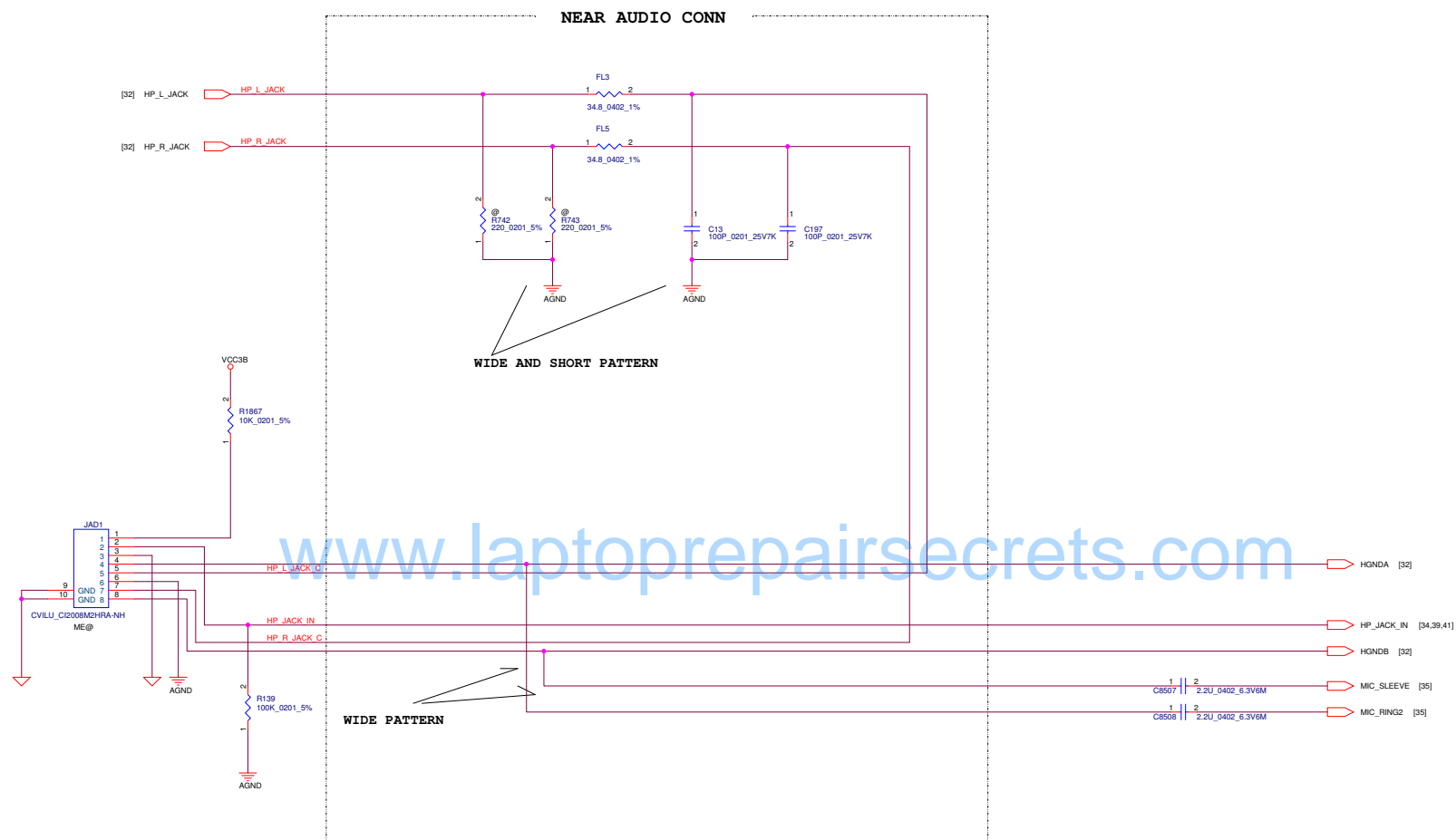
Security Classification	Compal Secret Data			Title
Issued Date	2014/11/04	Deciphered Date	2016/12/31	SMART CARD/FPR
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TABLE MIC HW ENABLE/DISABLE

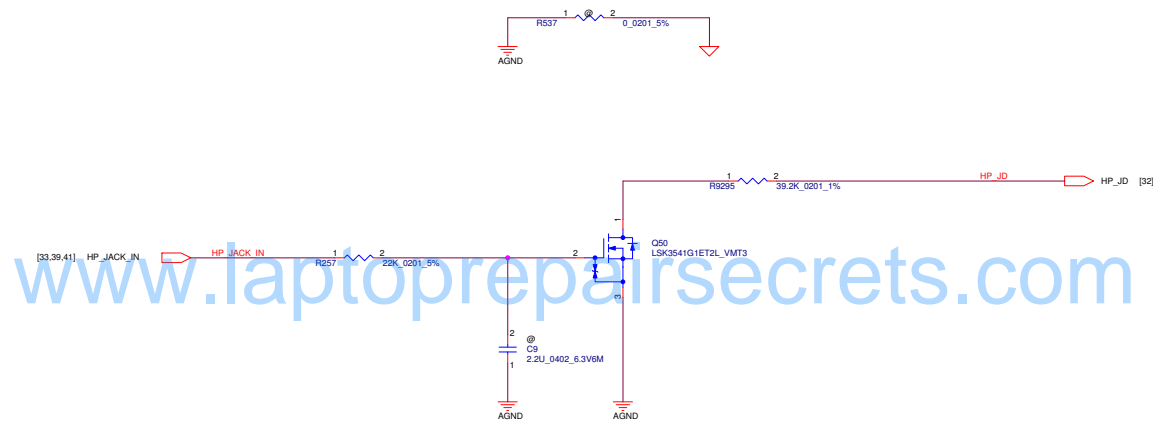
	ENABLE	DISABLE
R961	ASM	NO ASM
R119	ASM	NO ASM

LOGIC

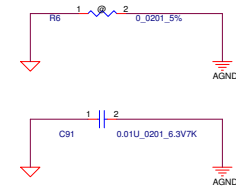
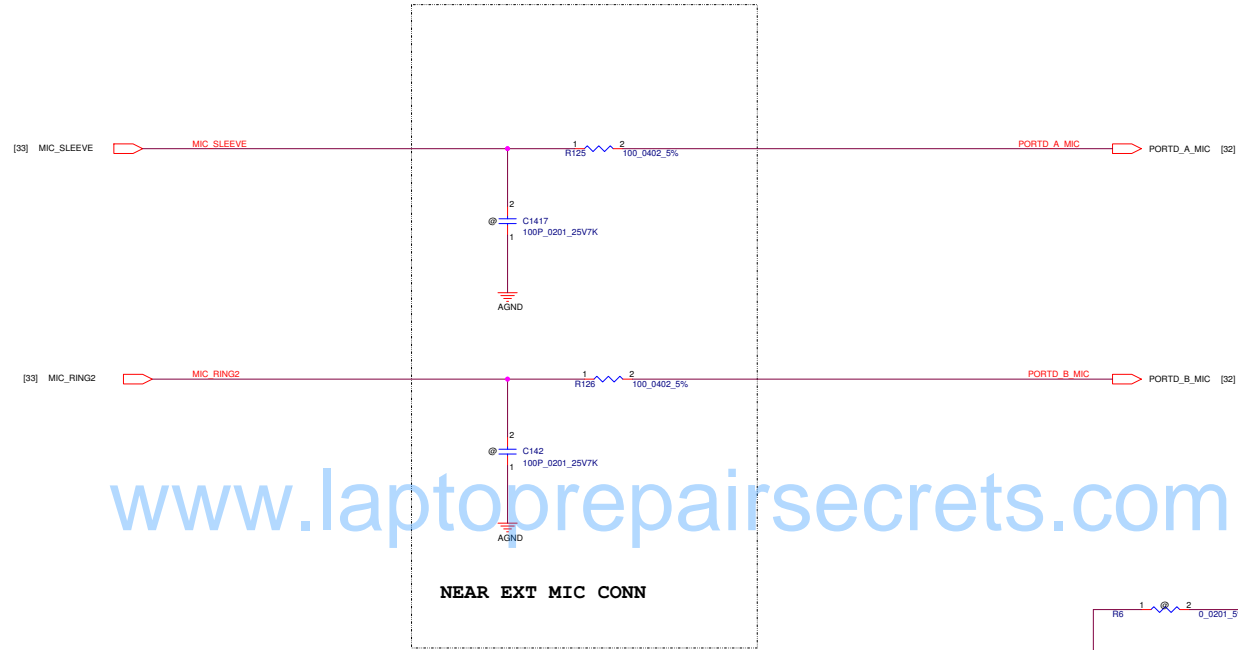




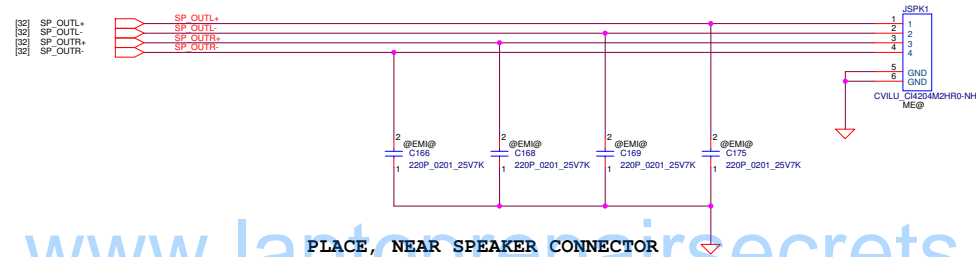
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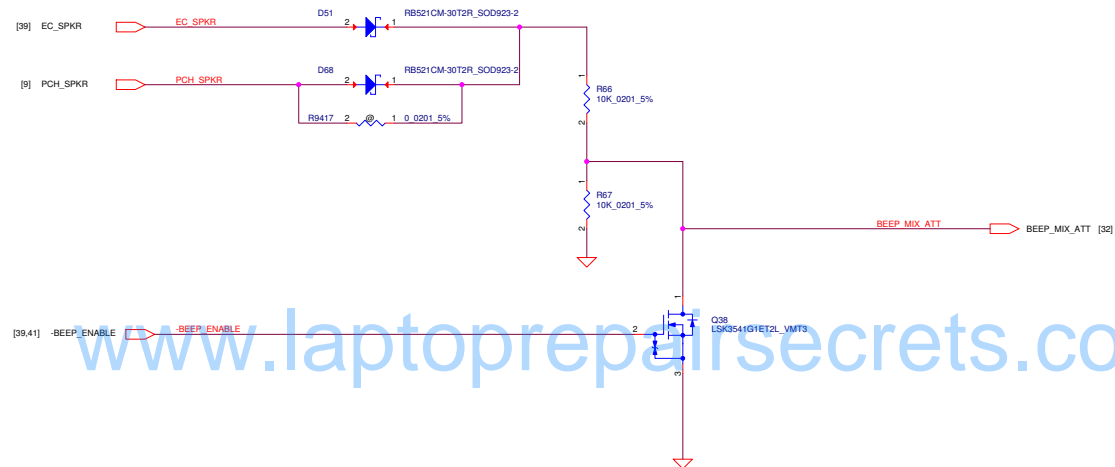


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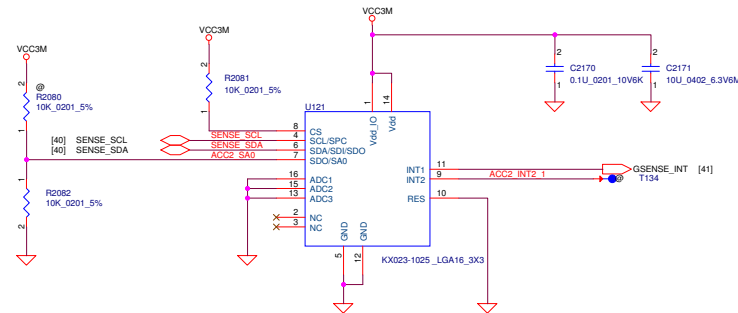
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AUDIO BEEP
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TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

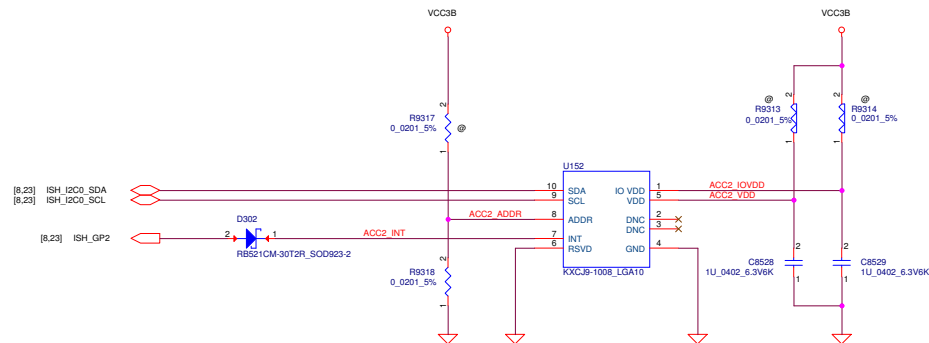
TABLE

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

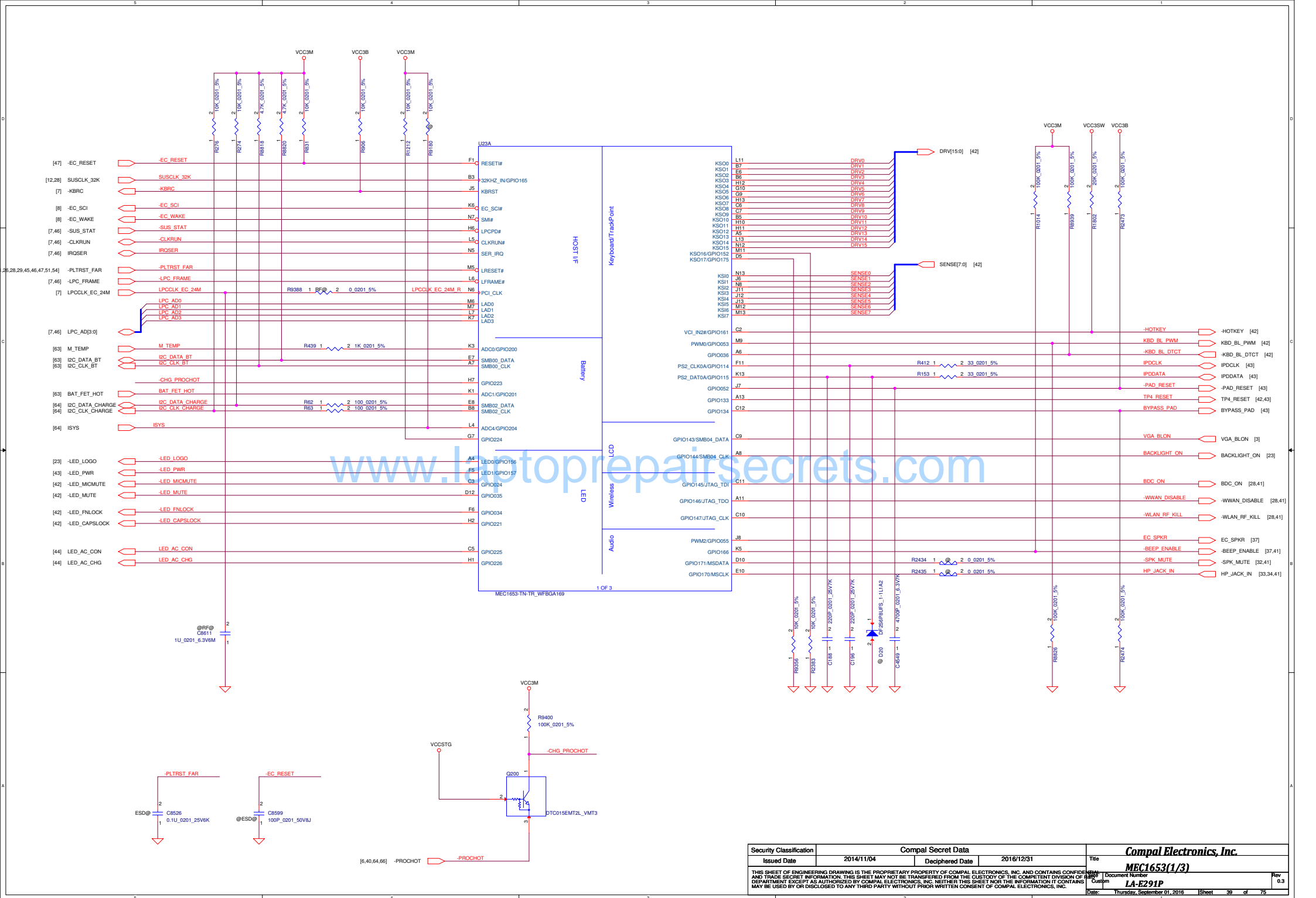


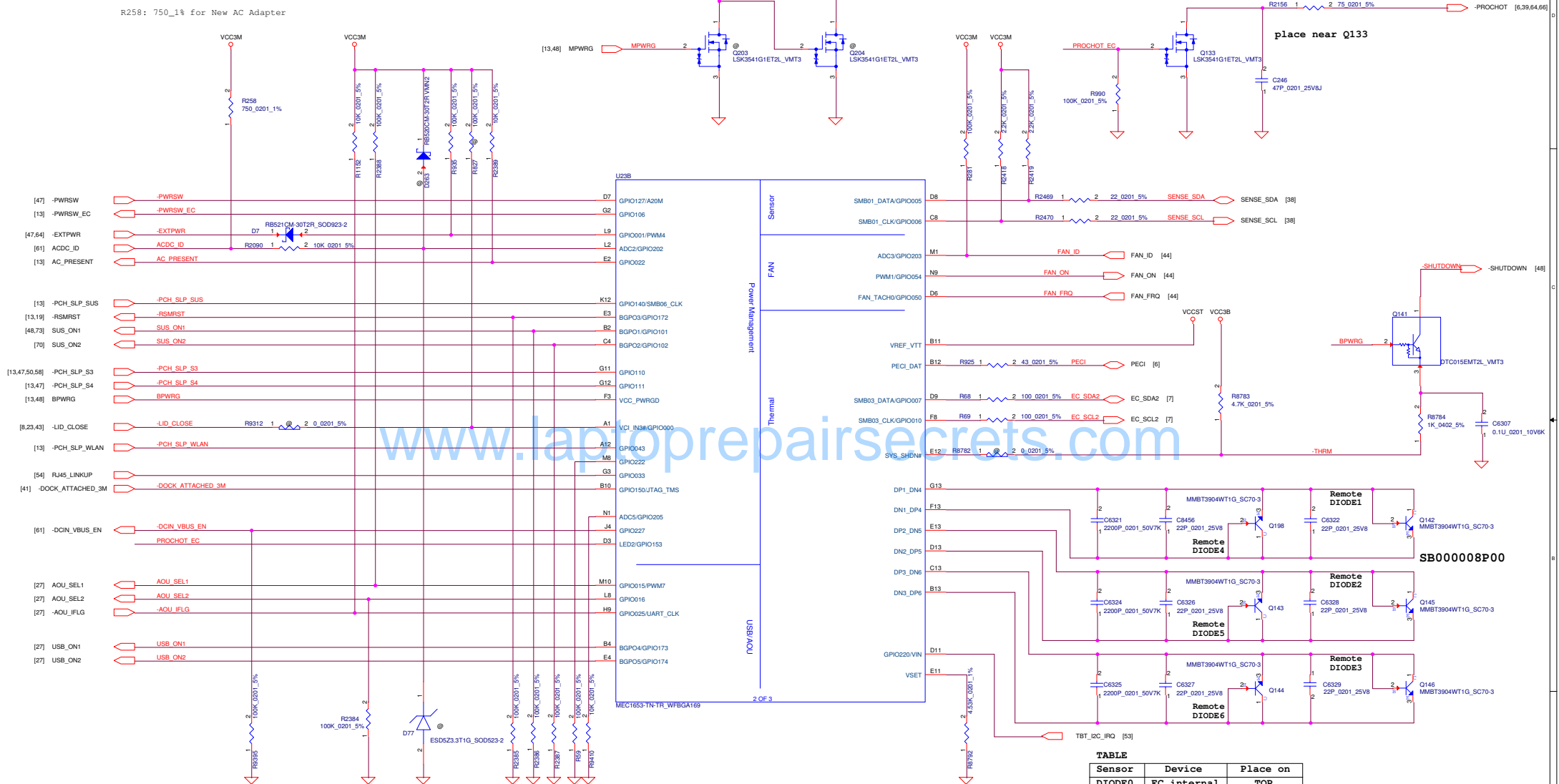
KX023-1025 Address: 0x1Eh

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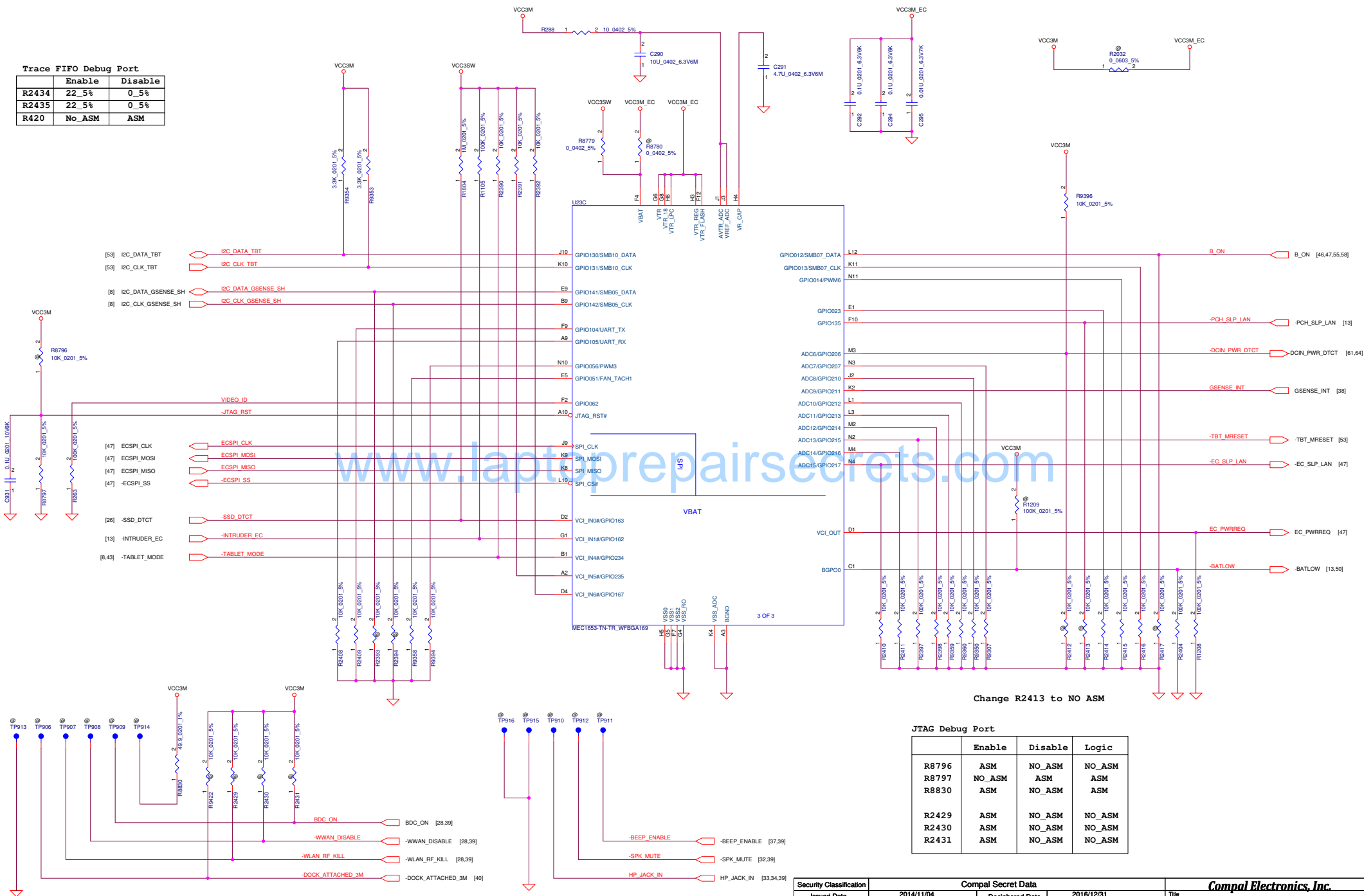
KXCJ9 Address: 0x1Ch





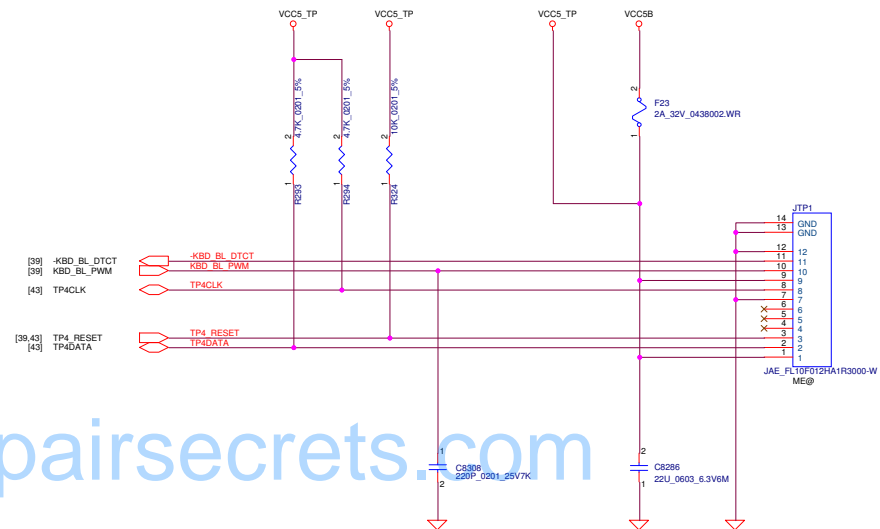
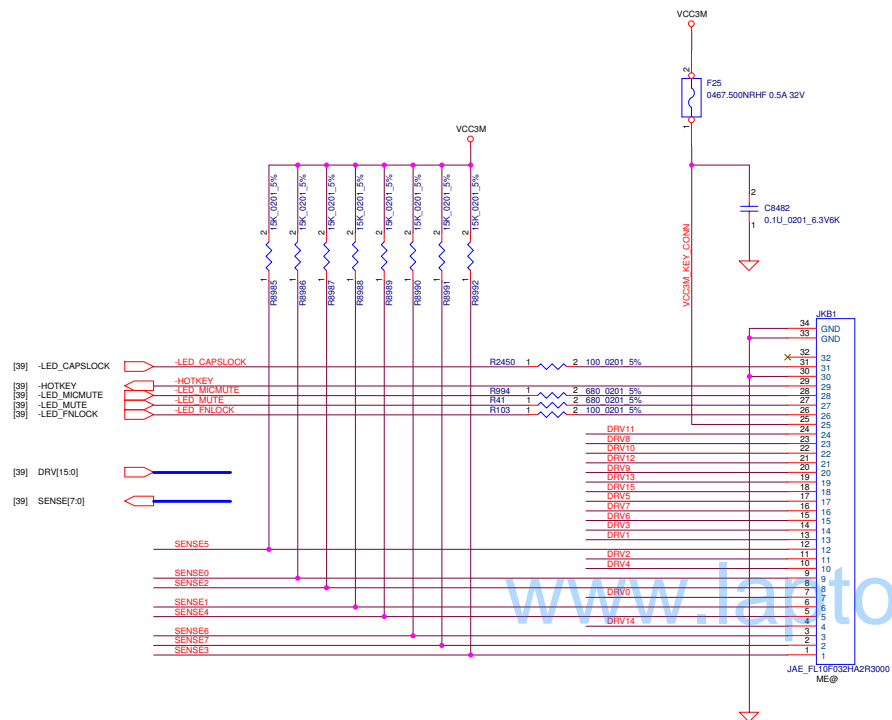
Sensor	Device	Place on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	SSD	BOTTOM
DIODE3	DIMM	BOTTOM
DIODE4	FAN/HEATPIPE	BOTTOM
DIODE5	WLAN/WWAN	BOTTOM
DIODE6	CHARGER	BOTTOM

Trace FIFO Debug Port		
	Enable	Disable
R2434	22.5%	0.5%
R2435	22.5%	0.5%
R420	No_ASM	ASM



JTAG Debug Port			
	Enable	Disable	Logic
R8796	ASM	NO_ASM	NO_ASM
R8797	NO_ASM	ASM	ASM
R8830	ASM	NO_ASM	ASM
R2429	ASM	NO_ASM	NO_ASM
R2430	ASM	NO_ASM	NO_ASM
R2431	ASM	NO_ASM	NO_ASM

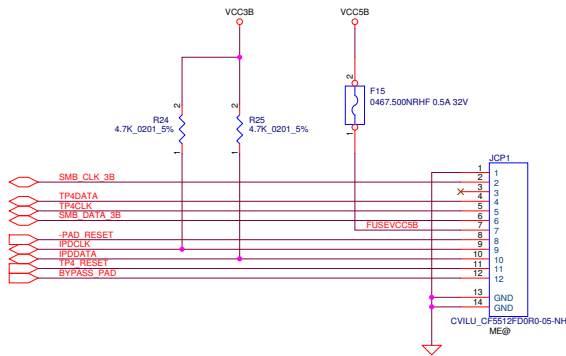
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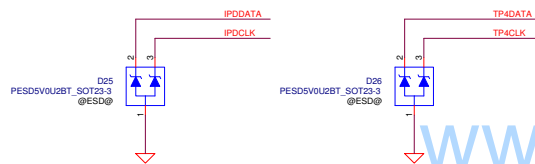
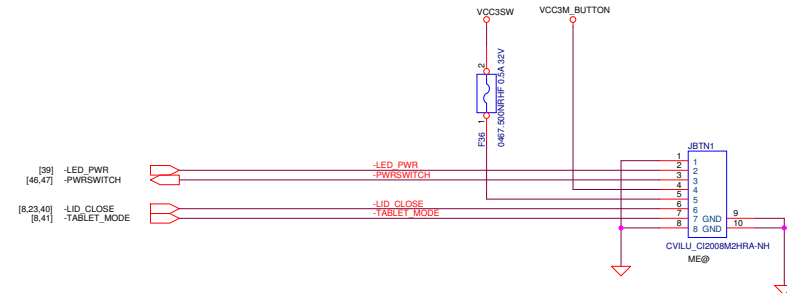
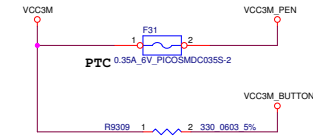
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Clickpad

- [21,46] SMB_CLK_3B
- [42] TP4DATA
- [42] TP4CLK
- [21,46] SMB_DATA_3B
- [39] -PAD_RESET
- [39] IPDCLK
- [39] IPDDATA
- [39,42] TP4_RESET
- [39] BYPASS_PAD

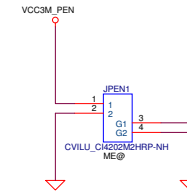
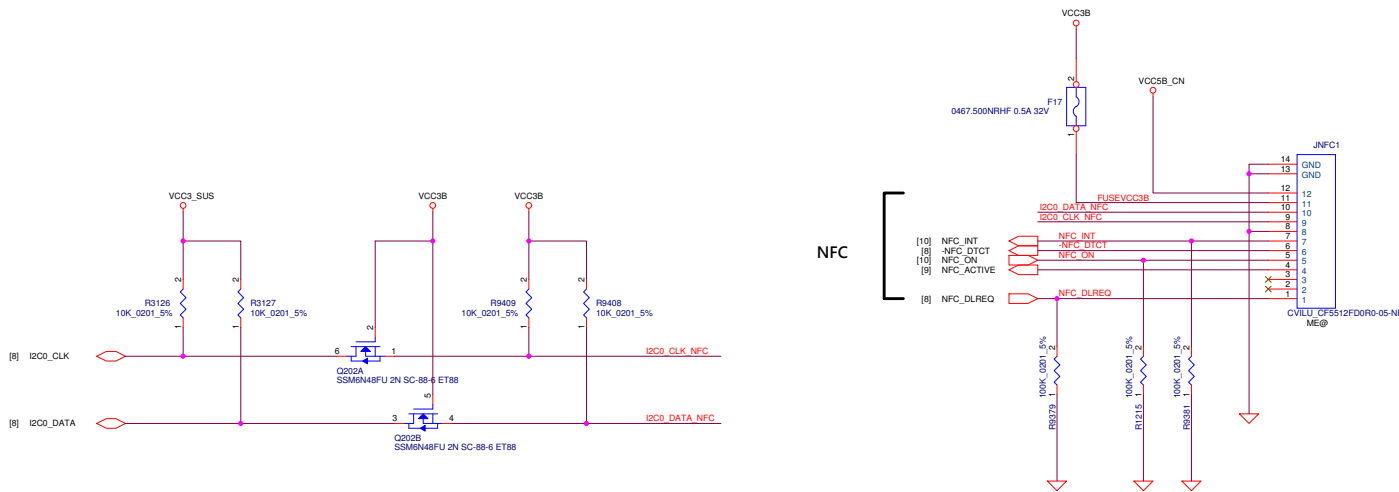


TO SUB BOARD

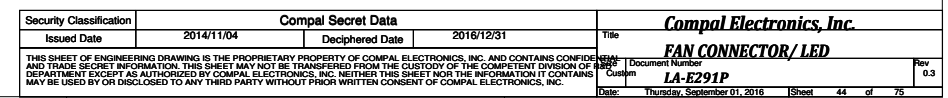


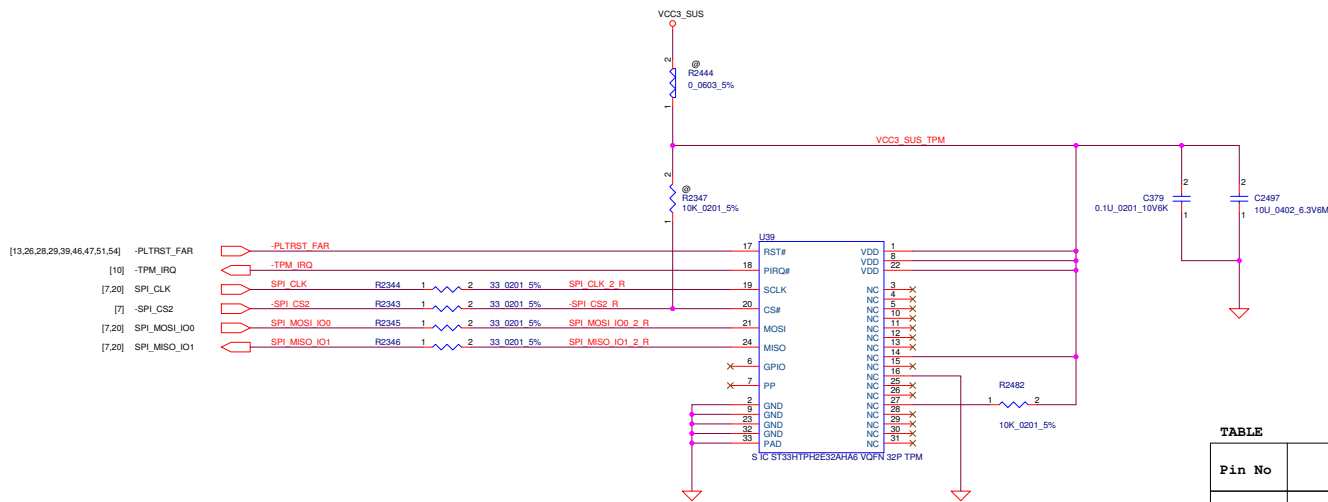
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NFC



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-Change TPM1.2 to TPM2.0
-Infineon SLB9670VQ2.0 part number SA00009N210
-ST ST33HPTH2E32AHA6 part number SA00009S010

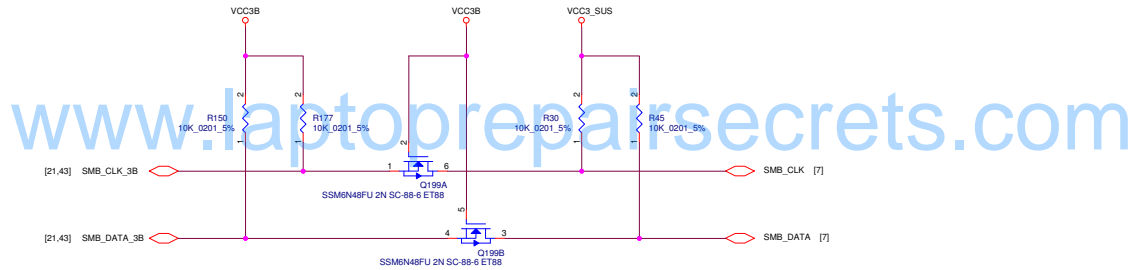
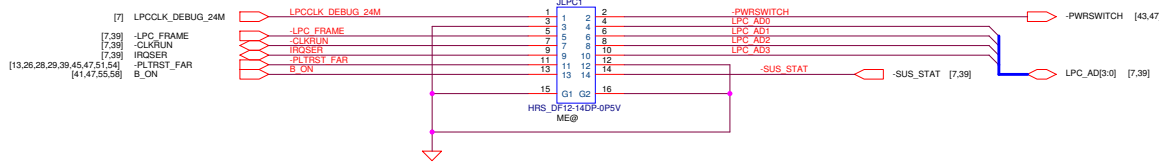
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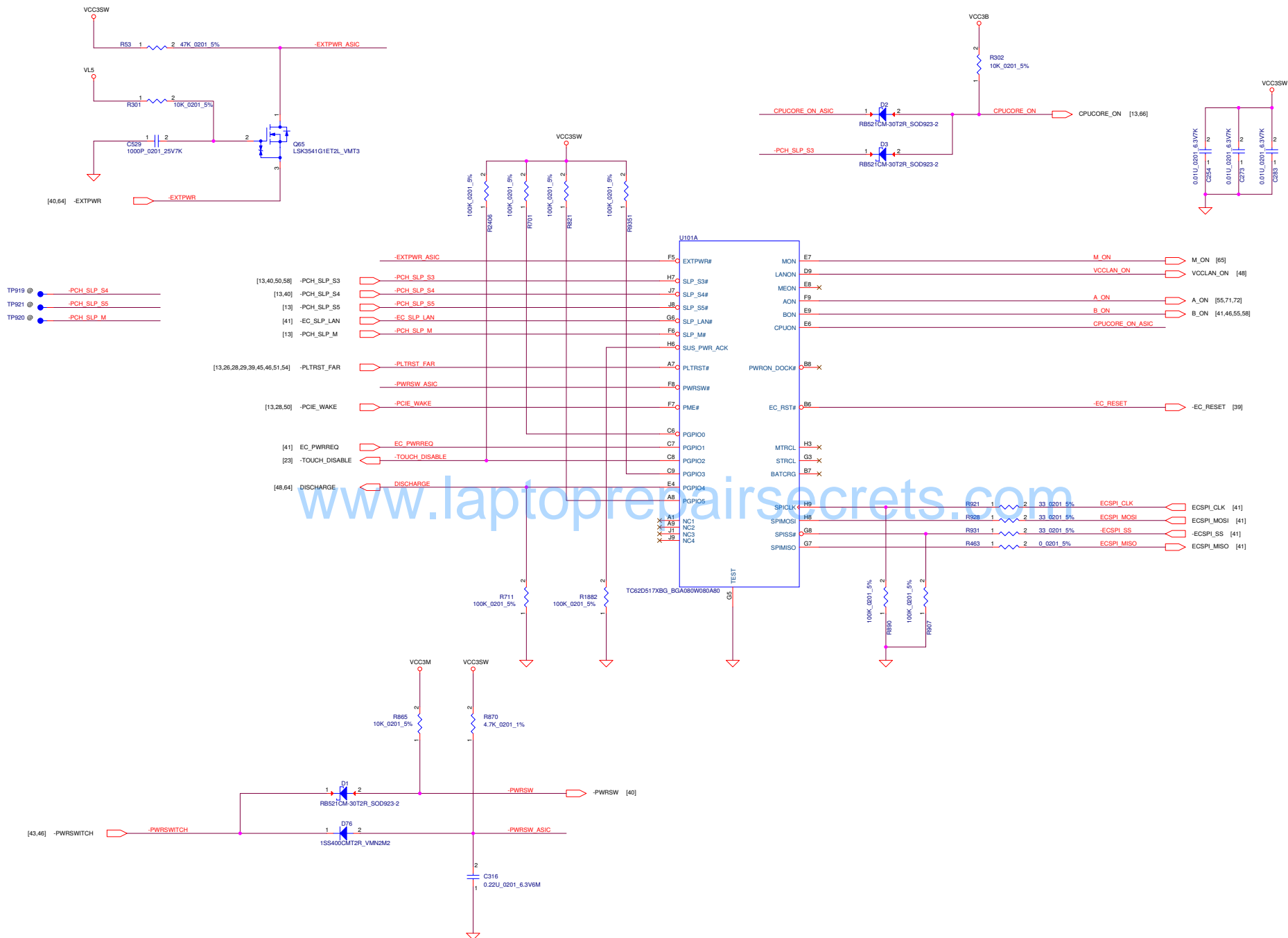
TABLE

Pin No	ST ST33HPTH2E32AHA6	Infineon SLB9670VQ2.0 FW7.60
1	NC	VDD
2	GND	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	GPIO
7	PP	PP
8	NC	VDD
9	NC	GND
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	VDD
15	NC	NC
16	NC	GND
17	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK
20	SPI_CS#	CS#
21	MOSI	MOSI
22	VDD	VDD
23	NC	GND
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	GND

TABLE			
REF	DES	ENABLE	DISABLE
JLPC1		ASM	NO_ASM
R220		ASM	NO_ASM

↑
LOGIC

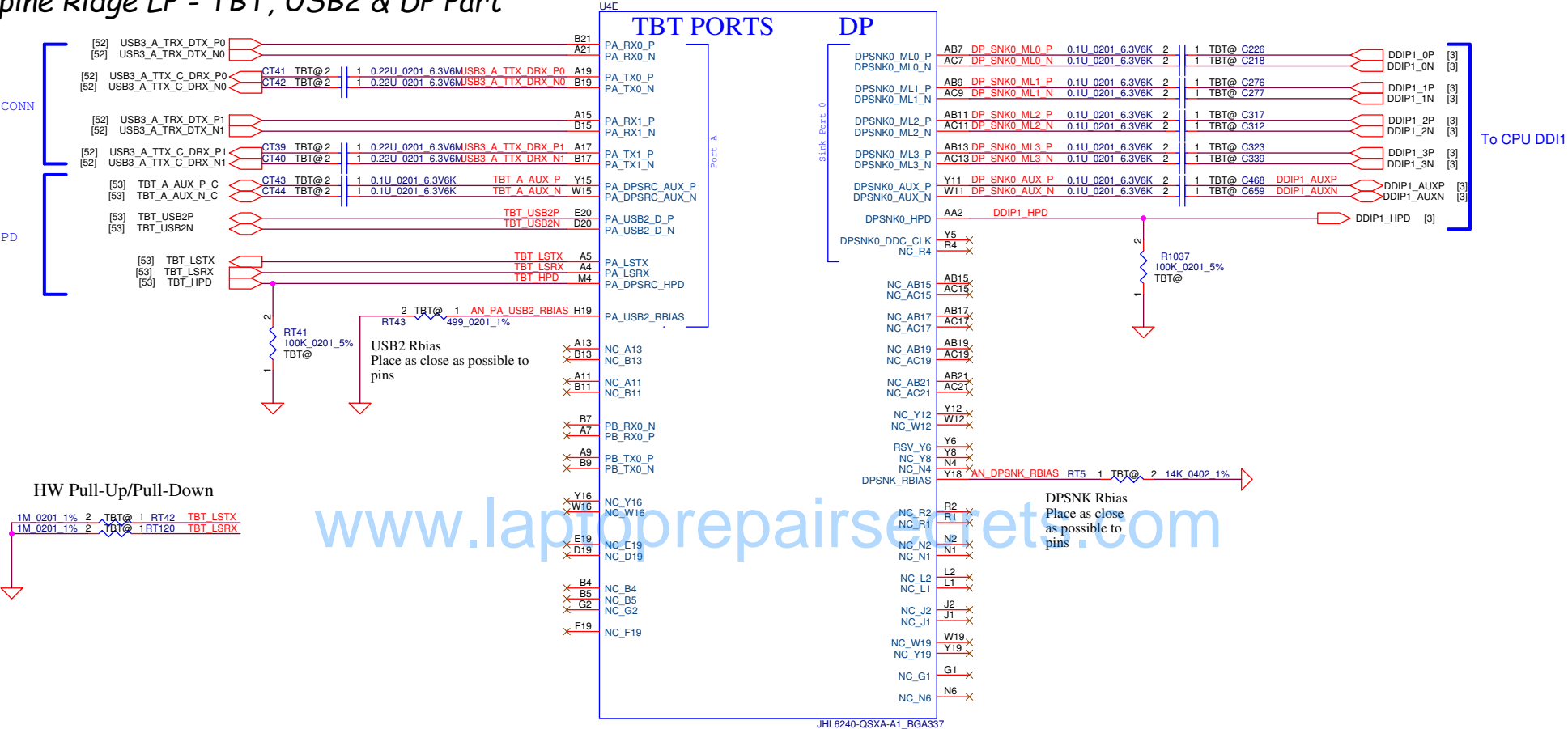


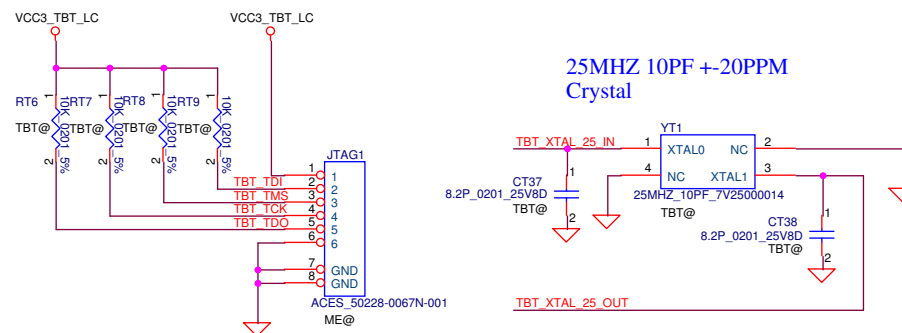
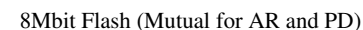
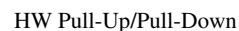


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Alpine Ridge LP - TBT, USB2 & DP Part

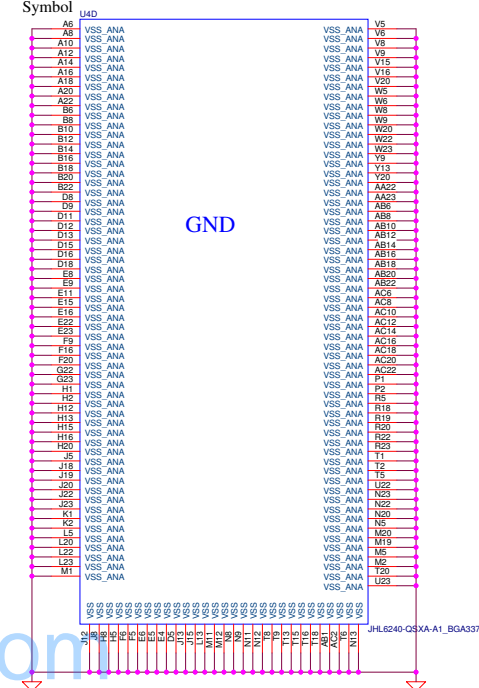
Alpine Ridge LP - TBT, USB2 & DP Part



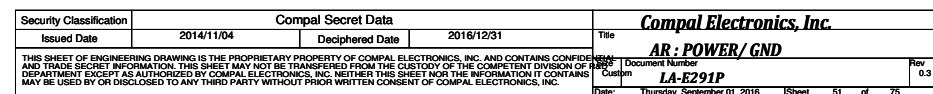
Alpine Ridge LP - Misc
Symbol

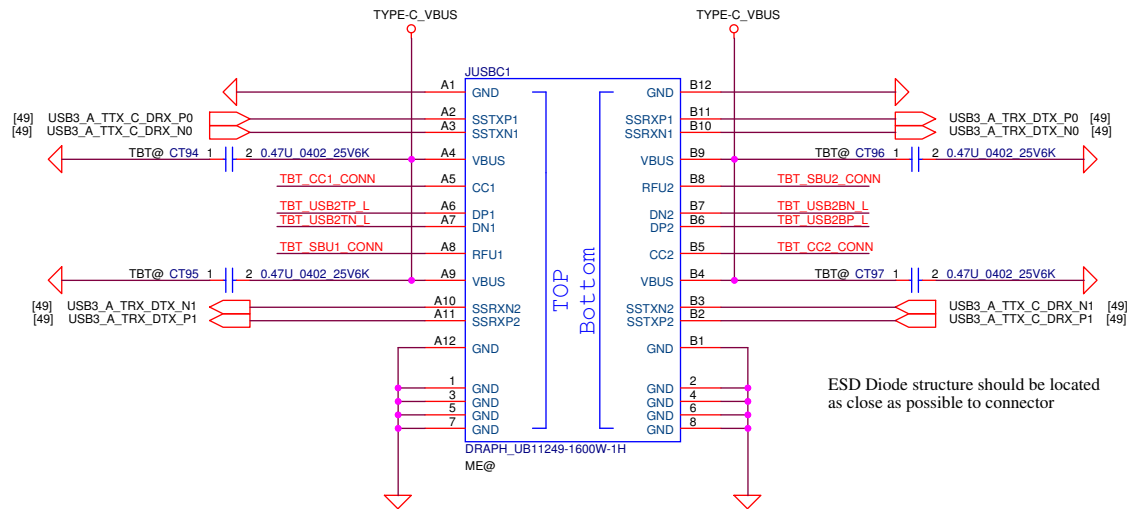
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Alpine Ridge SP - VCC
Symbol

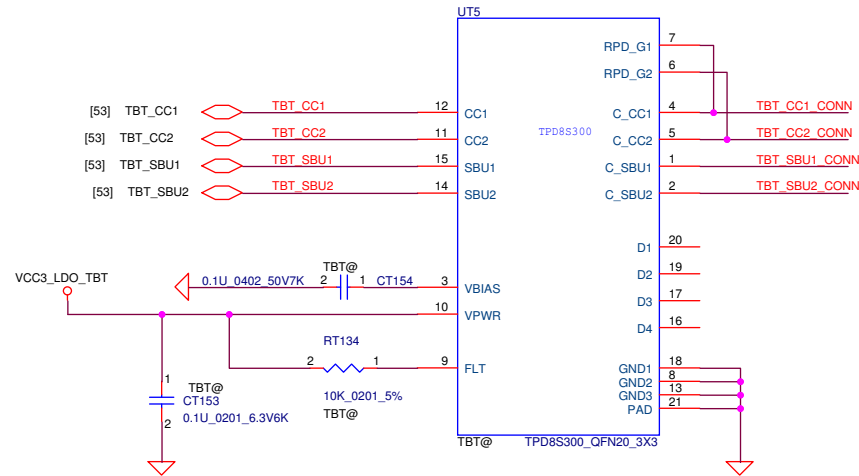
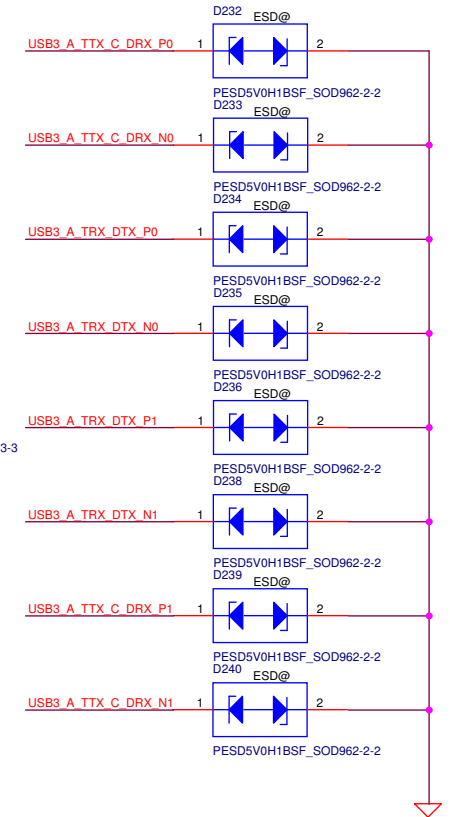
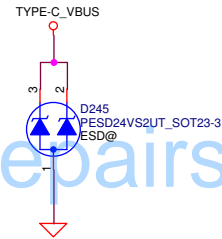
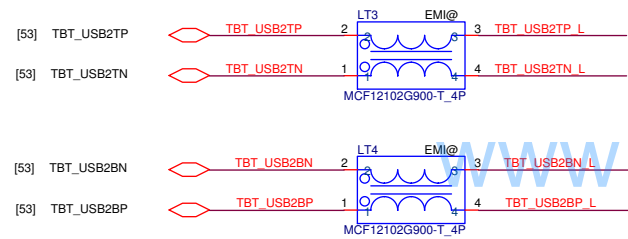
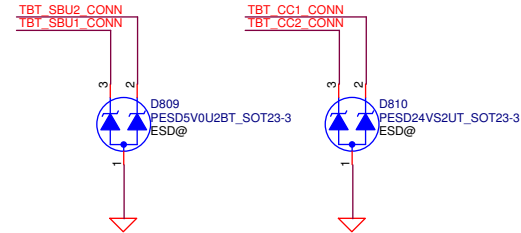
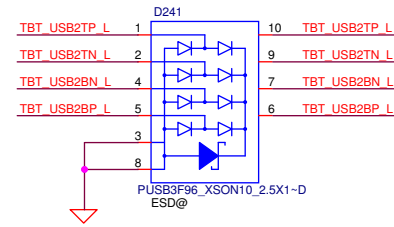
Symbol L4D

Symbol





ESD for USB2 Lines and Control lines



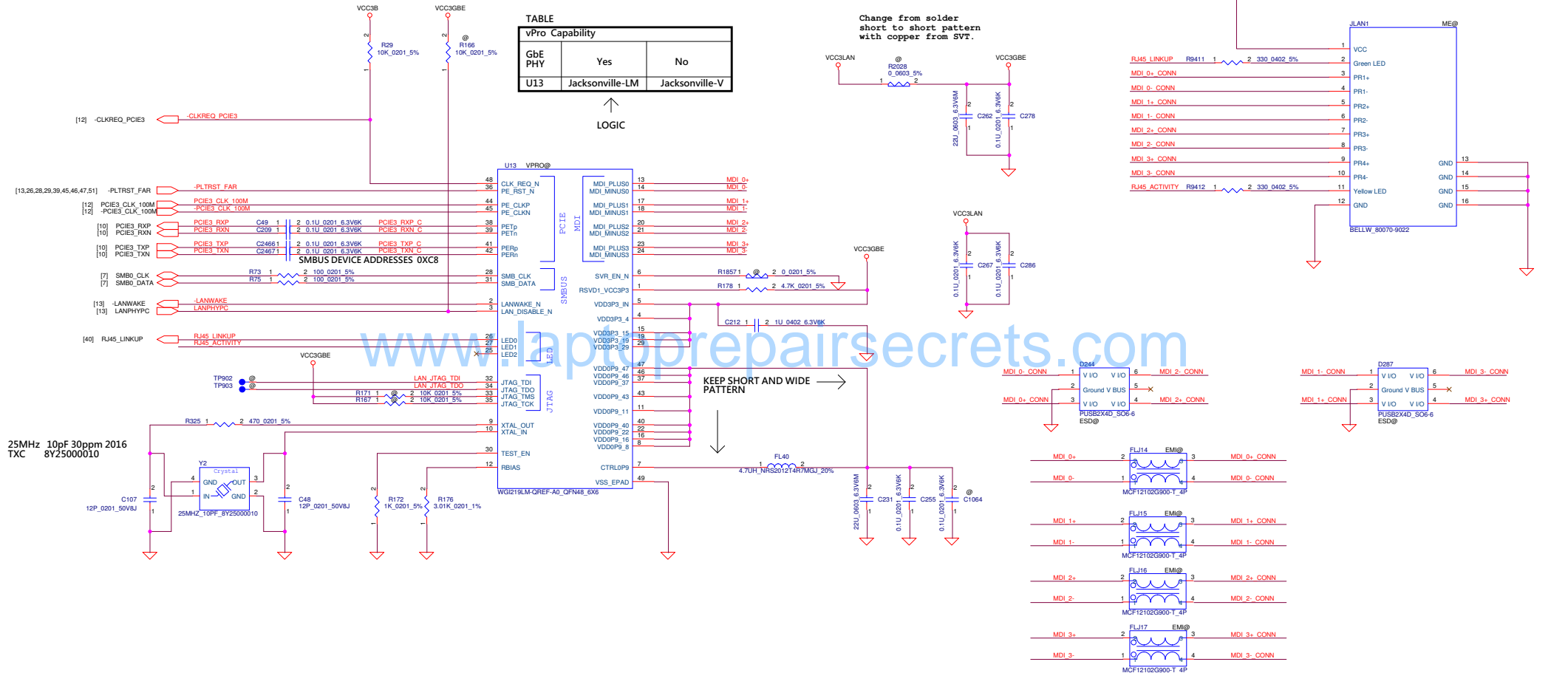
TBT_CC1 RT9354 1 @TBT@ 2 0.0201 5% TBT_CC1_CONN

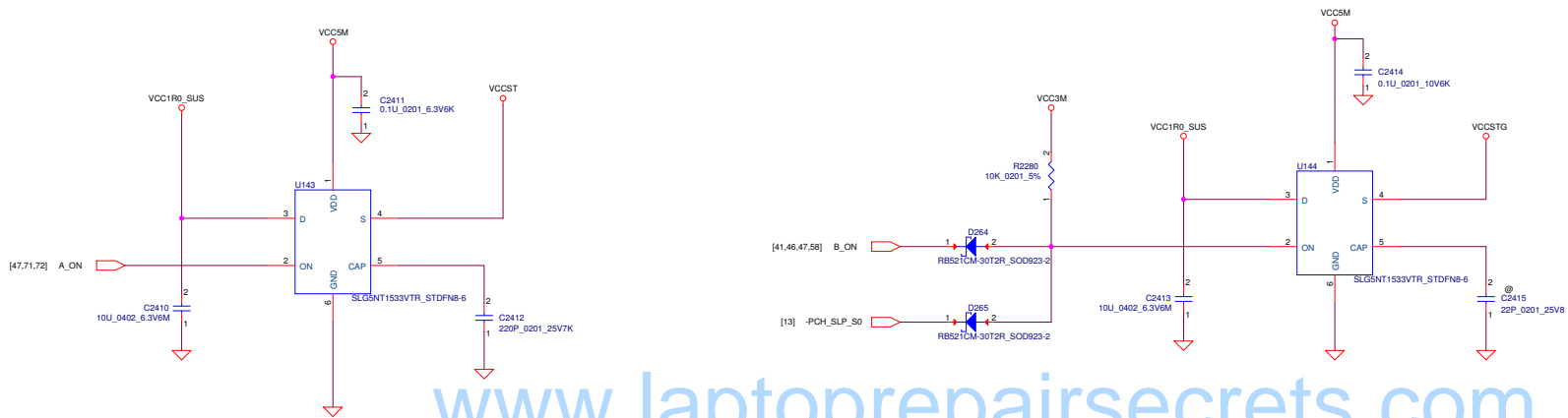
TBT_CC2 RT9355 1 @TBT@ 2 0.0201 5% TBT_CC2_CONN

TBT_SBU1 RT9356 1 @TBT@ 2 0.0201 5% TBT_SBU1_CONN

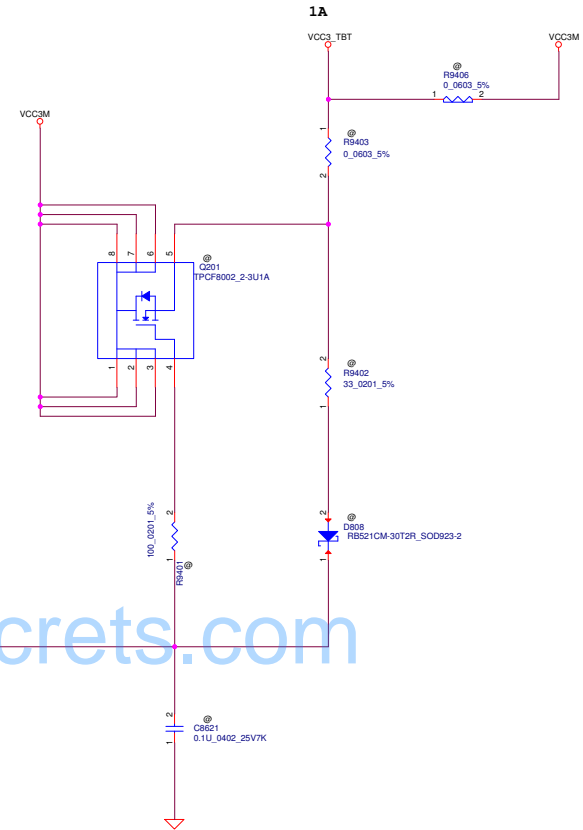
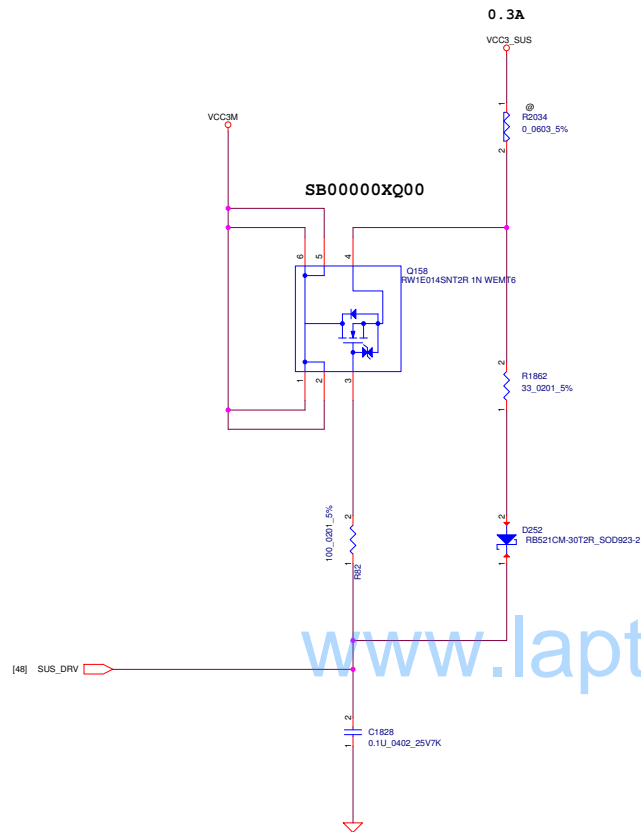
TBT_SBU2 RT9357 1 @TBT@ 2 0.0201 5% TBT_SBU2_CONN

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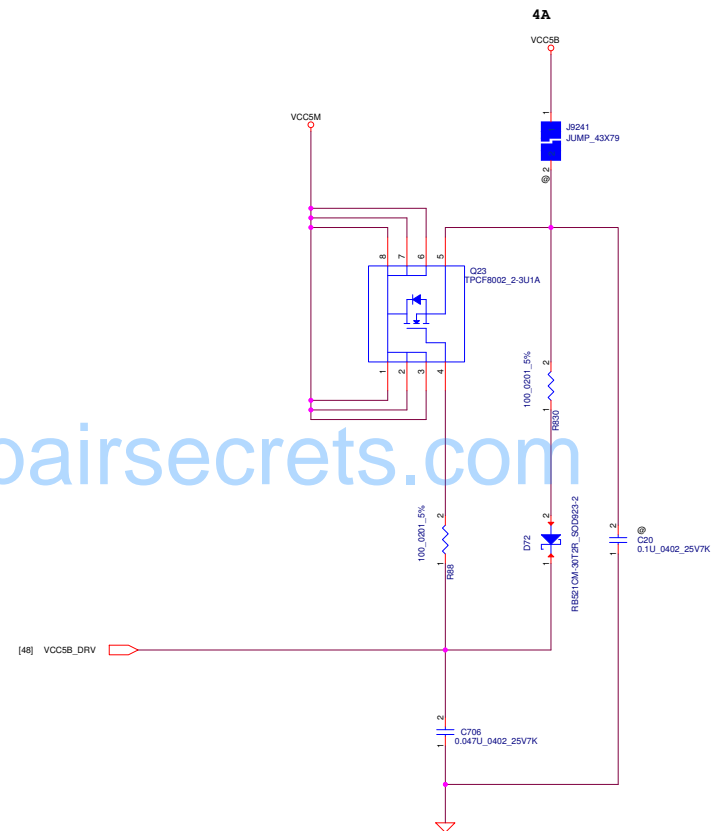
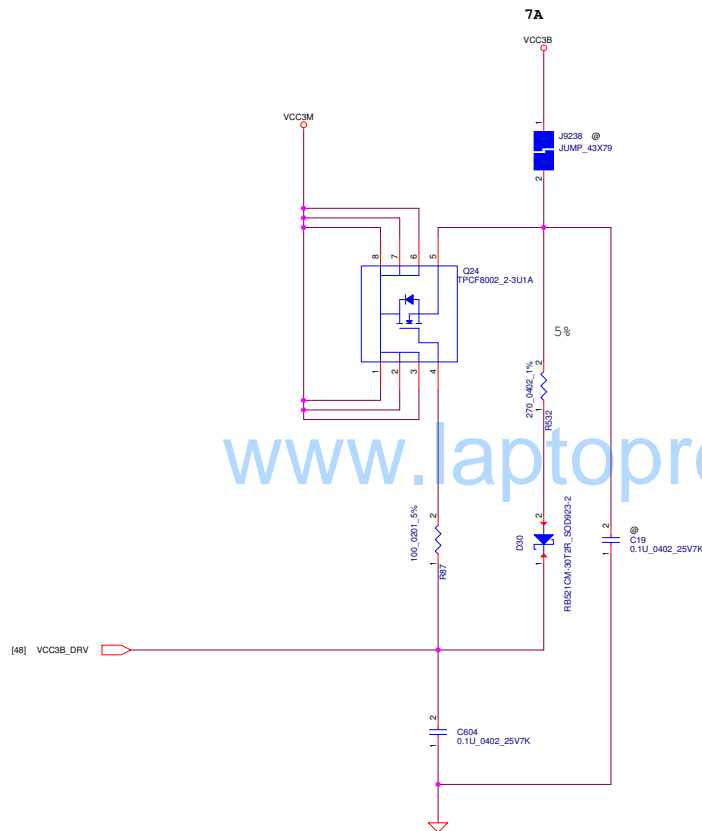




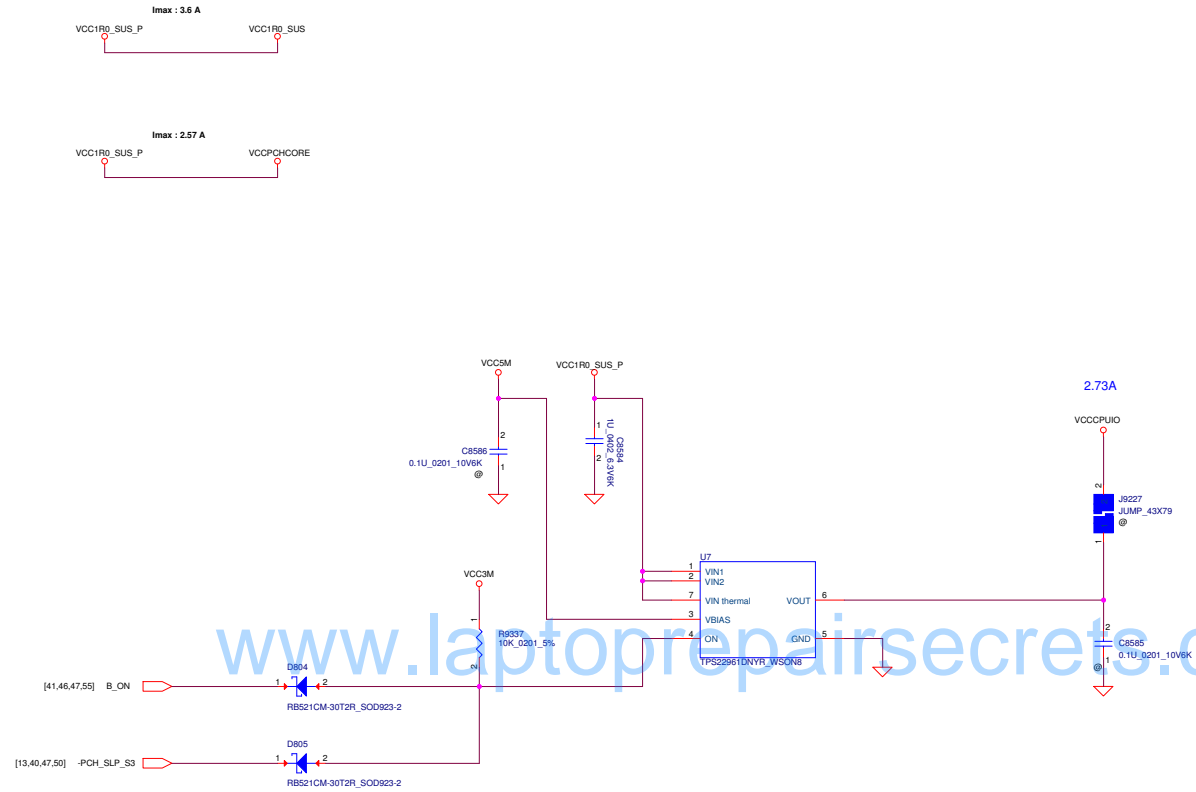
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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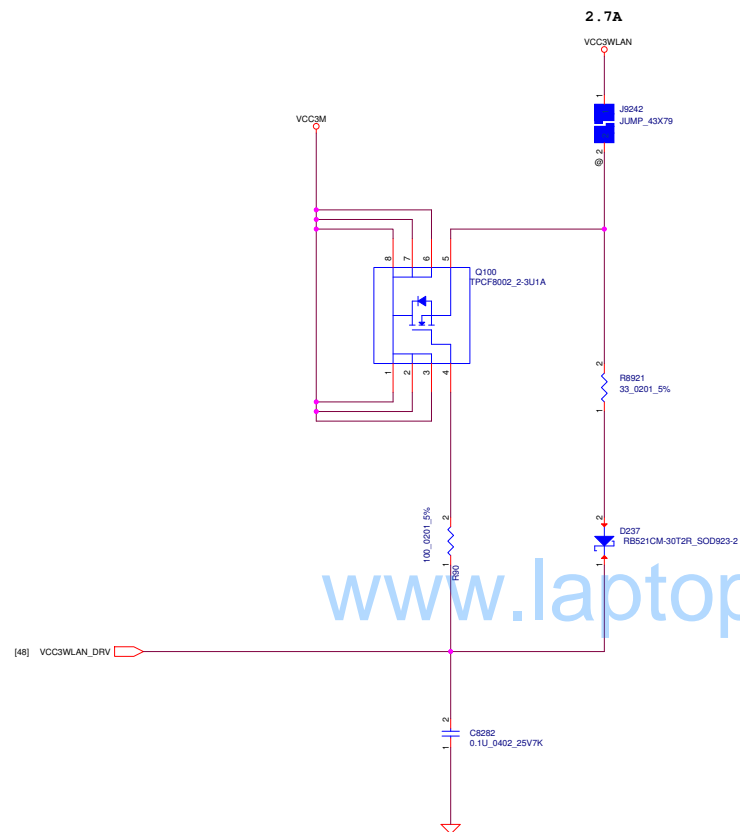
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				Date	Thursday, September 01, 2016
				Sheet	57 of 75
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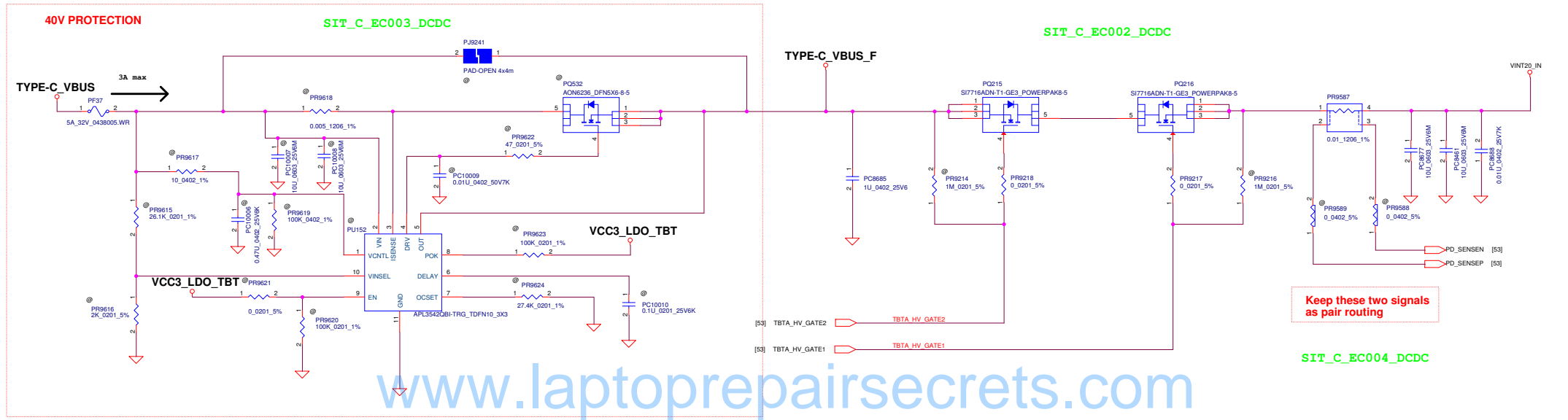


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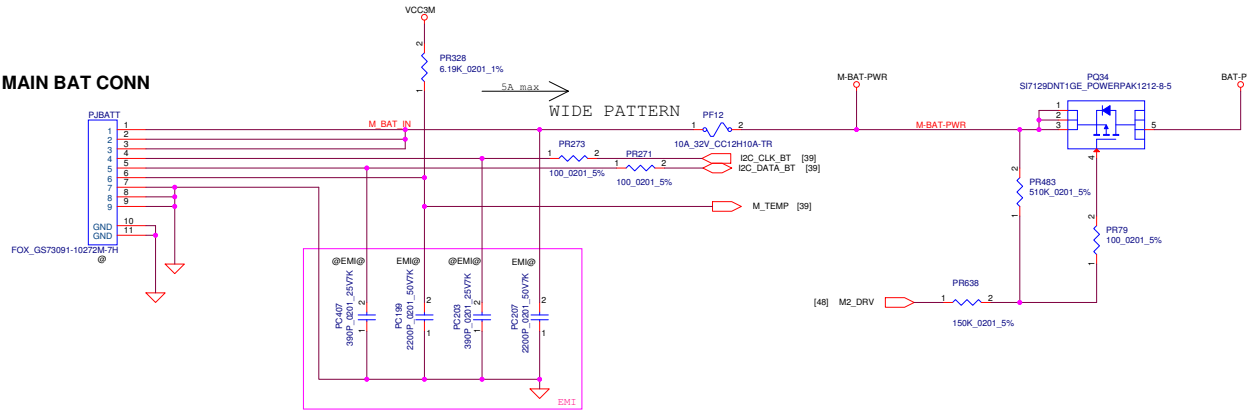
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				Date	Thursday, September 01, 2016
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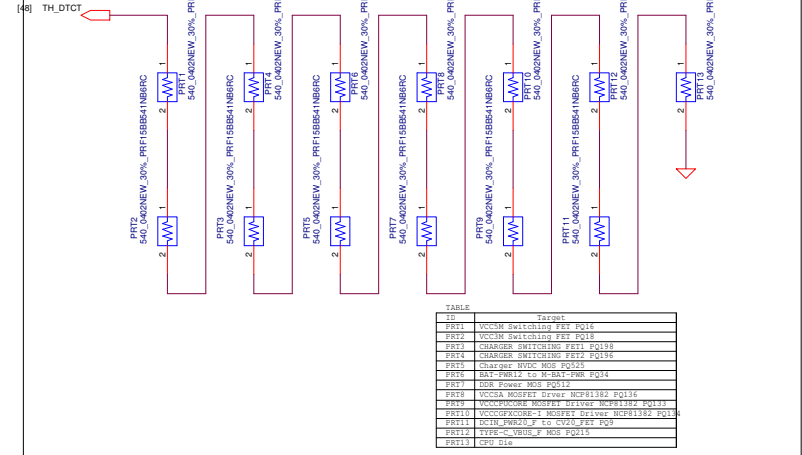


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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title
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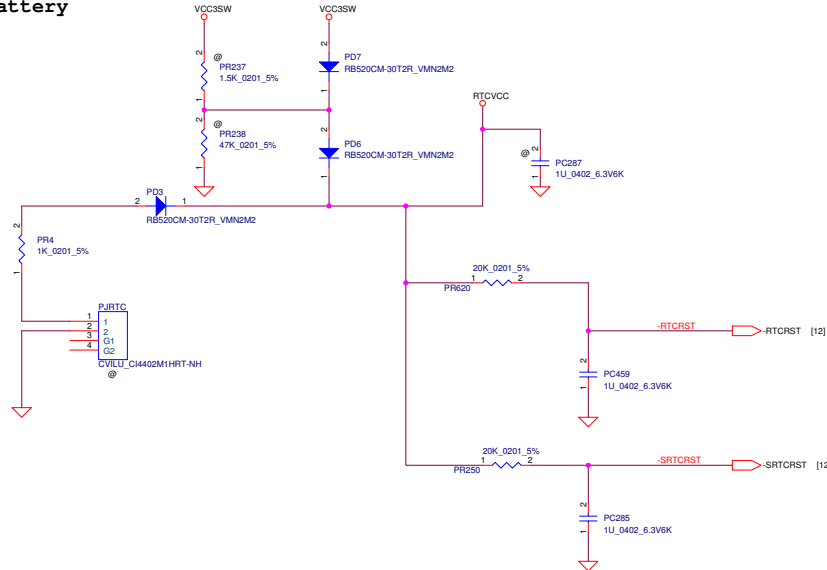
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PTC function

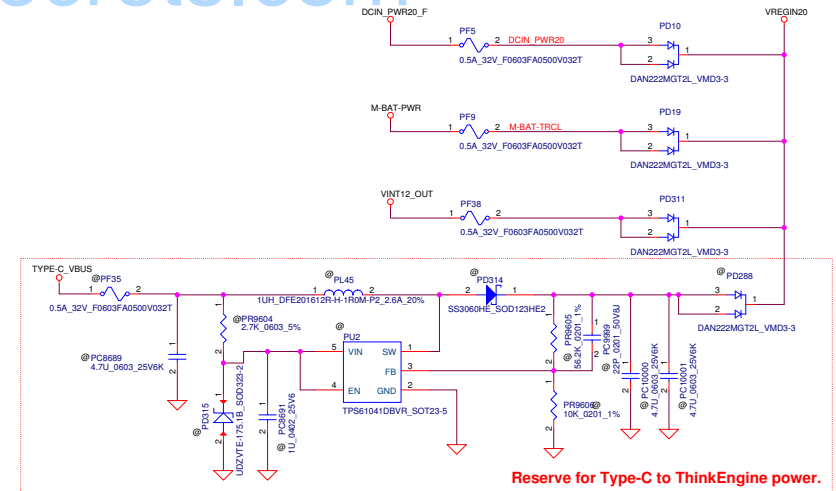


RTC Battery

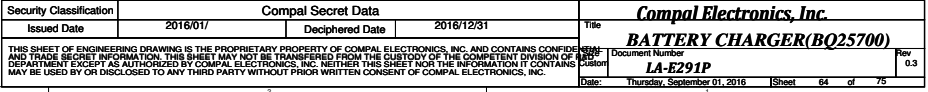


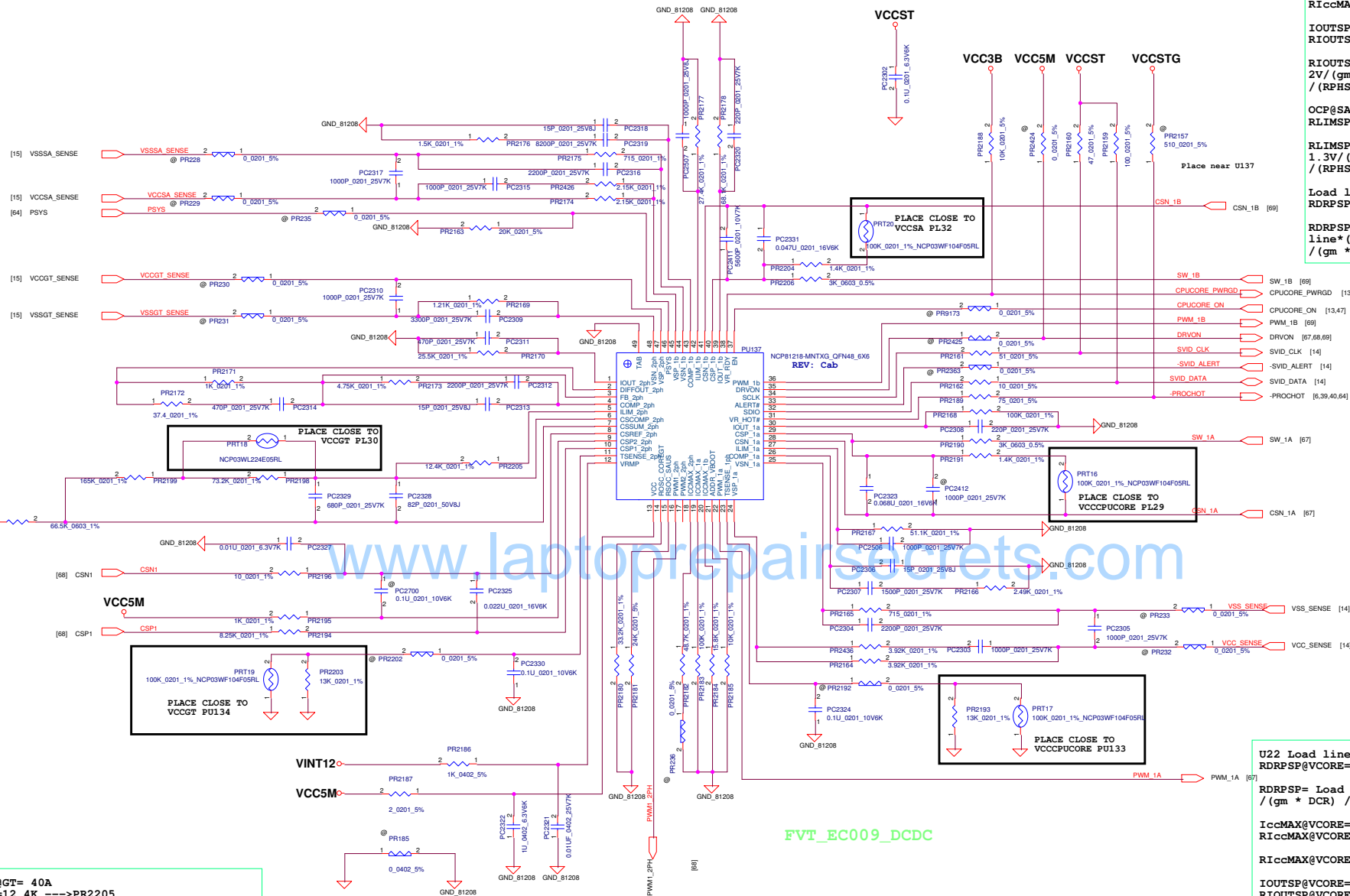
FVT_EC003_DCDC

Power to ThinkEngine



Reserve for Type-C to ThinkEngine power.





U22 OCP@GT= 40A
 RLIM@GT=12.4K ---->PR2205
 RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
 RIccMAX2ph= 48.7K ---->PR2182
 RIccMAX2ph= (IccMAX2ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
 RIOUT@GT=25.5K ---->PR2170

RIOUT= 2* RLIM / (10 *IOUTICMAX * Load line)

U22 Load line@GT= 3.1m
 RPH@GT=84.5K ---->PR2130,PR2138

Load line= (RCS2+(RCS1*Rth)/(RCS1+Rth))
 *IOUTTOTAL * DCR/RPH

TABLE OCP

PR2167	51.1K	Ilim=40A	VCCCPUCORE
PR2205	12.4K	Ilim=40A	VCCGFXCORE
PR2177	27.4K	Ilim=10A	VCCSA

SIT_C_EC004_DCDC
 SIT_C_EC005_DCDC

FVT_EC009_DCDC

IccMAX@SA= 5A
 RIccMAX@SA= 15.8K ---->PR2184

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
 RIOUTSP@SA=84.5K ---->PR2178

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICMAX*DCR / (RPHSP+Rth+RCSSP))

OCP@SA= 10A
 RLIMSP@SA=27.4K ---->PR2177

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR / (RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
 RDRPSP@SA=2.15K ---->PR2174

RDRPSP= Load line*(RPHSP+Rth+RCSSP) / (gm * DCR) / (Rth+RCSSP)

U22 Load line@VCORE= 2.35m
 RDRPSP@VCORE=3.92K ---->PR2436

RDRPSP= Load line*(RPHSP+Rth+RCSSP) / (gm * DCR) / (Rth+RCSSP)

IccMAX@VCORE= 32A
 RIccMAX@VCORE= 100K ---->PR2183

RIccMAX@VCORE= IccMAX*2V/10uA/64A

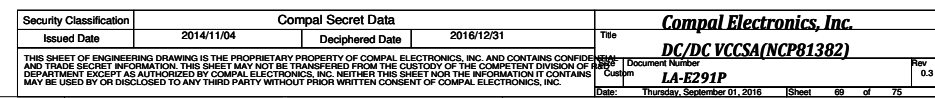
IOUTSP@VCORE= 32A
 RIOUTSP@VCORE=100K ---->PR2168

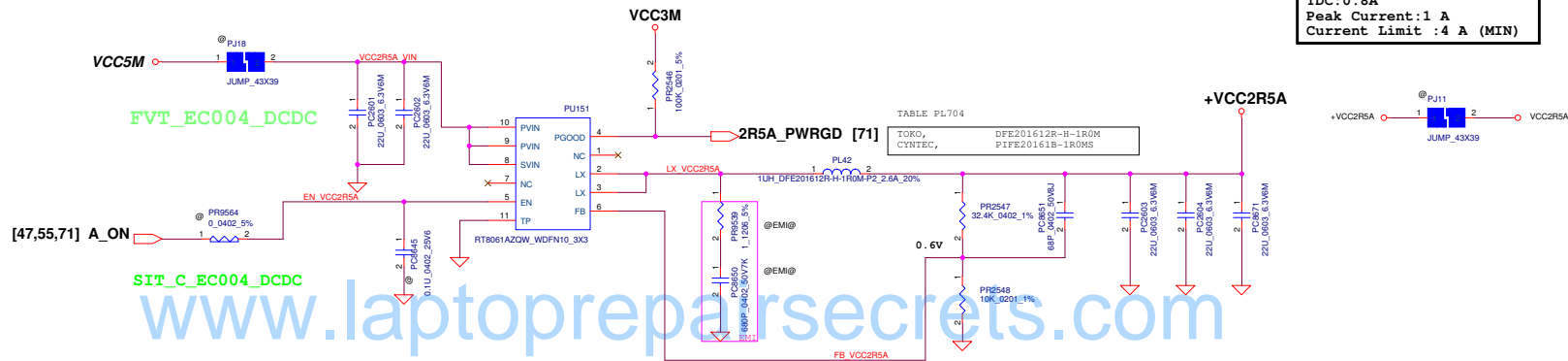
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICMAX*DCR / (RPHSP+Rth+RCSSP))

OCP@VCORE= 40A
 RLIMSP@VCORE=51.1K ---->PR2167

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR / (RPHSP+Rth+RCSSP))

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Compal Electronics, Inc. DC/DC IMVP6 CONTROLLER				LA-E291P
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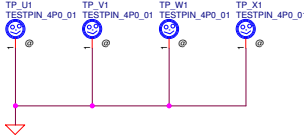
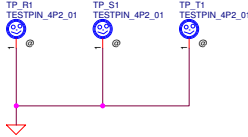
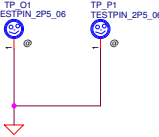
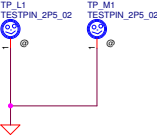
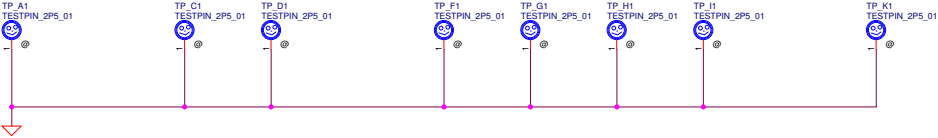




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PTH FOR SCREW HOLE

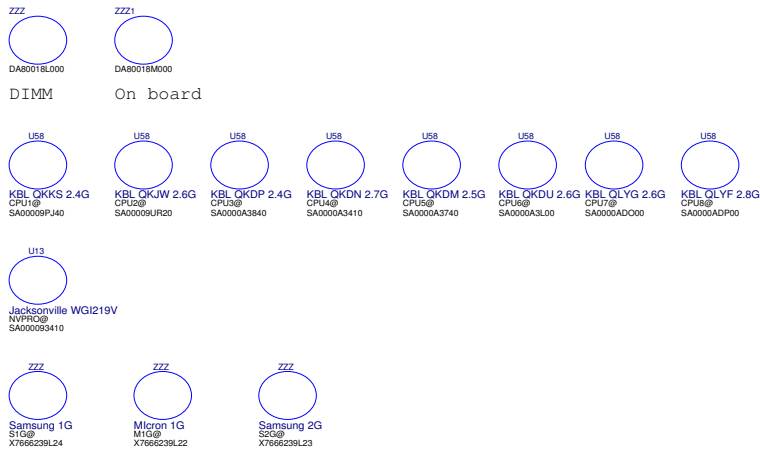
Value	Hole Dia	Pad Dia		QTY
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	9
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



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FID
Board Area





BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO LAN chip	VPRO@	WGI219LM
non vPRO LAN chip	NVPRO@	WGI219V
Thunderbolt requirement	TBT@	
Thunderbolt reserve	@TBT@	
ESD requirement	ESD@	
ESD reserve	@ESD@	
EMI requirement	EMI@	
EMI reserve	@EMI@	
RF requirement	RF@	
RF reserve	@RF@	
XDP	XDP@	
On board RAM	X76@	

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